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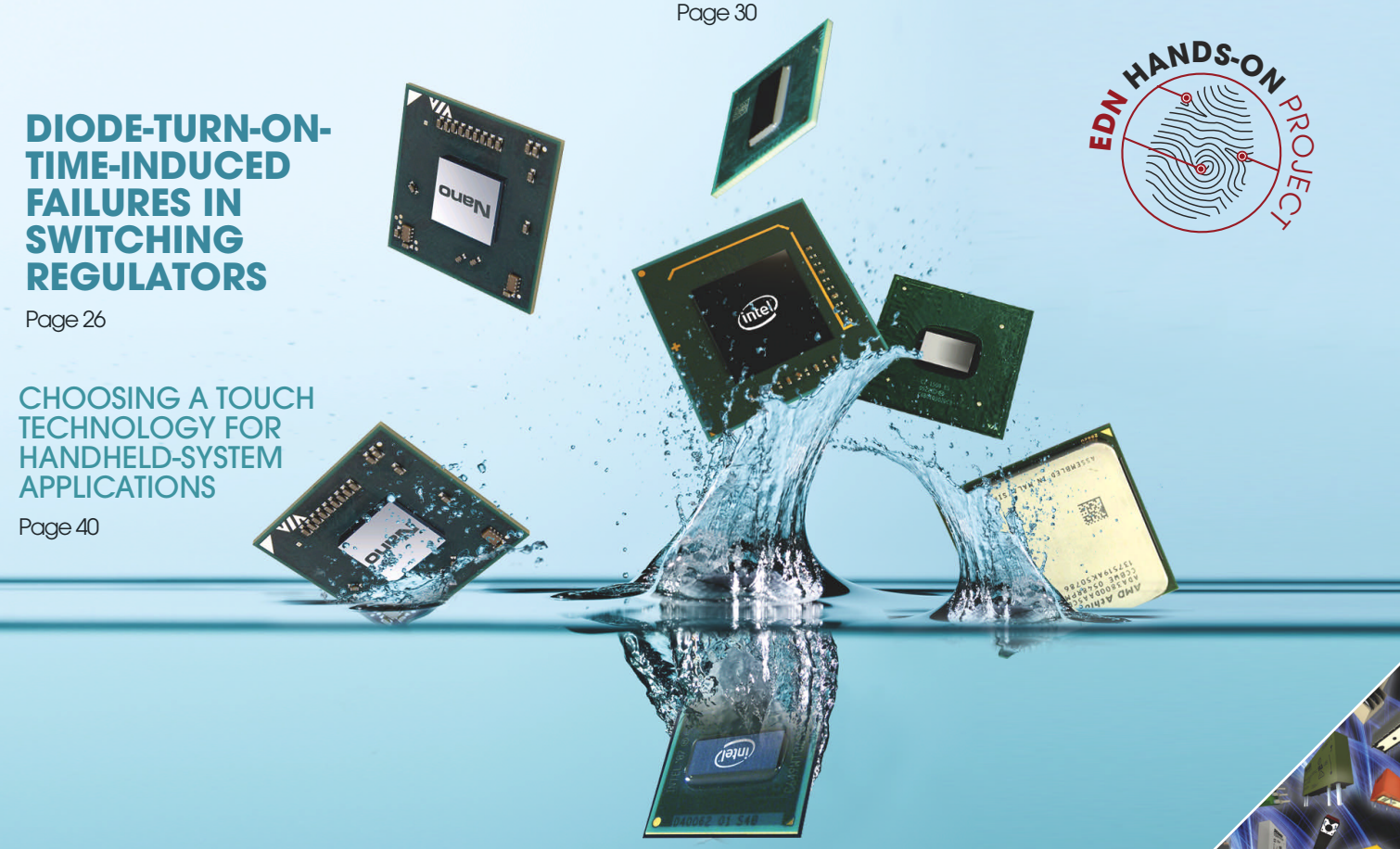

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Product	Erasable Sector	Speed	Density
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M25PX	4 KB, 64 KB	75 MHz (Dual I/O)	8 Mb - 64 Mb
M25/M45PE	256 B, 4 KB, 64 KB	50 MHz, 75 MHz	1 Mb - 16 Mb

EMBEDDED PARALLEL NOR FLASH MEMORY

Product	Voltage	Performance	Density
J3 v.D	2.7V - 3.6V	X8, X16 Page	32 Mb - 256 Mb
P30	1.7V - 2.0V, 1.7V - 3.6V	X16 52 MHz Burst	64 Mb - 512 Mb
P33	2.3V - 3.6V	X16 52 MHz Burst	64 Mb - 512 Mb
M29W†	2.7V - 3.6V	X8, X16 Page	4 Mb - 128 Mb
M58BW†	2.7V - 3.6V, 2.5V - 3.3V (55ns)	X32 Burst	16 Mb - 32 Mb

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Product	Voltage	Page Size	Density
SLC small page	1.8V/3V	512 B	128 Mb – 1 Gb
SLC large page	1.8V/3V	2 KB	1 Gb - 8 Gb
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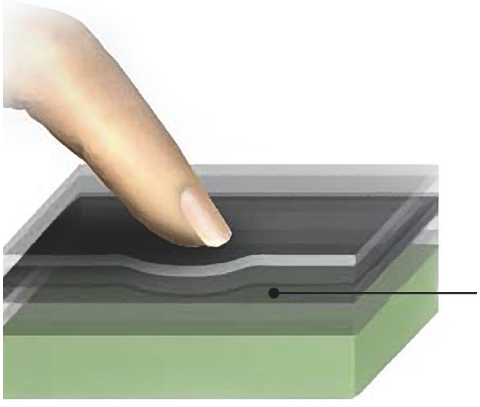
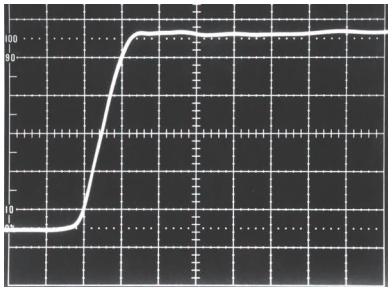
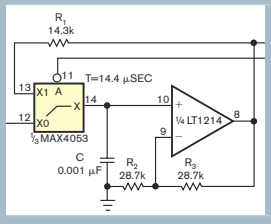


The price of falling prices: evaluating value-oriented x86 CPUs



Diode-turn-on-time-induced failures in switching regulators

DESIGNIDEAS



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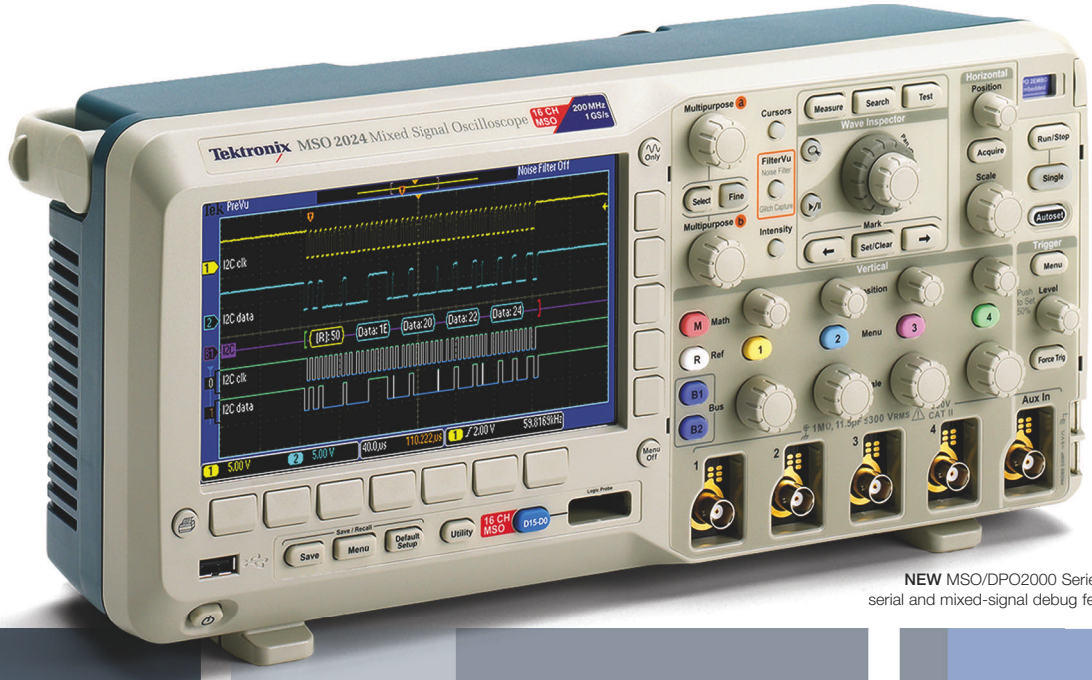

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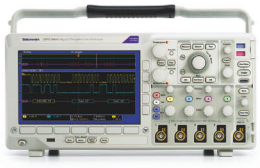
Bandwidth	350 MHz to 1 GHz
Analog Channels	2, 4
Digital Channels	16 (MSO4000 Series)
Record Length	10 M on all channels
Display	10.4 inch
Serial Bus Trigger and Decode	I²C, SPI, RS-232/422/485/UART, CAN, LIN, FlexRay



DPO3000 Series	
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Analog Channels	2, 4
Digital Channels	—
Record Length	5 M on all channels
Display	9.0 inch
Serial Bus Trigger and Decode	I²C, SPI, RS-232/422/485/UART, CAN, LIN

NEW! MSO2000/DPO2000 Series	
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Digital Channels	16 (MSO2000 Series)
Record Length	1 M on all channels
Display	7.0 inch
Serial Bus Trigger and Decode	I²C, SPI, RS-232/422/485/UART, CAN, LIN

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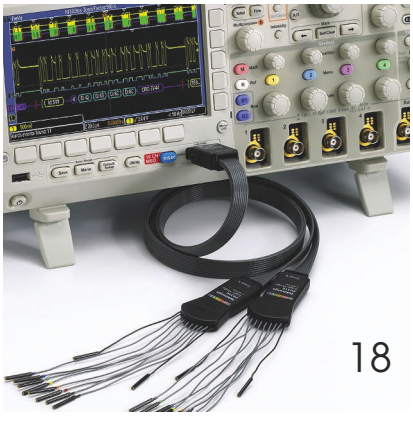

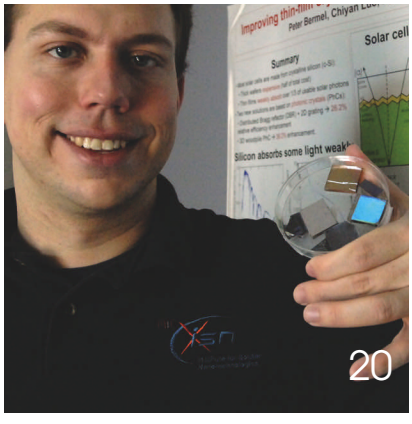

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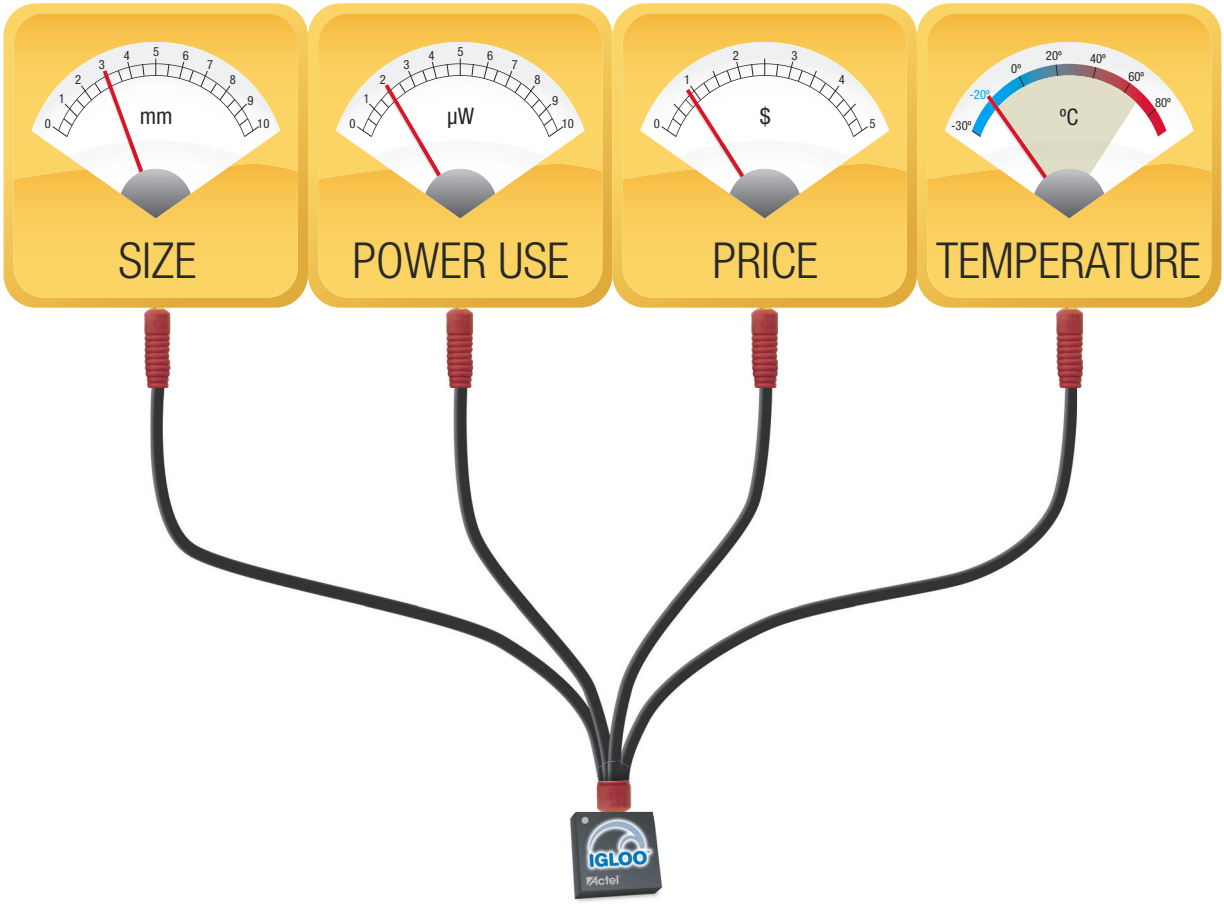

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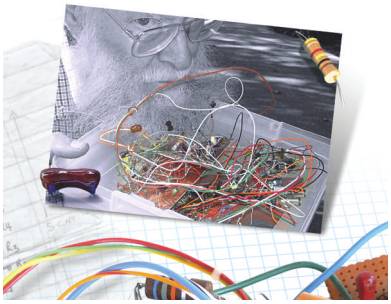

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BY BRIAN DIPERT, SENIOR TECHNICAL EDITOR

A bad idea that just won't die

In just over a month, barring a last-minute change of plans by the FCC (Federal Communications Commission) or another government entity, full-power, over-the-air analog television transmissions will cease in the United States. Despite my past cynical forecasts to the contrary, broadcast-flag restrictions will not plague the ATSC (Advanced Television Systems Committee) digital transmissions that currently coexist in many parts of this country and that will fully supersede their NTSC (National Television System Committee) predecessors on Feb 17. But this news does not vanquish the bigger-picture restriction aspirations of content-rights holders, which the broadcast flag exemplifies.

The broadcast flag is control data embedded in an ATSC bit stream that informs a receiver whether the content can move from one device to another, whether you can record it, or both, as well as any restrictions on the transport and recording. Although the US courts eventually ruled that the FCC had overstated its charter in insisting on broadcast-flag requirements, the damage arguably had already been done. Many television stations had purchased broadcast-flag-supportive transmission equipment. Several generations' worth of consumer-electronics gear support broadcast-flag specifications, too, and the equipment's intentionally locked firmware prevents the removal of this no-longer-necessary support.

Consumers' uproar over the broadcast flag occurred in general because content-rights owners insisted on restricting longstanding fair-use rights in the analog era, rights that consumers naively believed had been permanently codified following the 1984 decision in the case of Sony Corp of America versus Universal City Studios Inc, commonly known as the Betamax case. In actuality, the Digital Millennium Copyright Act nullified many of the Betamax-case provisions. And any early-adopter consumer who'd bought an expensive early-generation HDTV (high-definition television) without an HDCP (high-bandwidth-digital-content-protection)-augmented digital input or, for that matter, an expensive ATSC set-top box without an encryption-enhanced digital output no longer would be able to enjoy HDTV in the broadcast-flag era.

The broadcast flag may be extinct from an ATSC standpoint, but it has re-emerged in the form of selectable output control. Today, movies and other high-value video material are released to various venues in chronological order from most to least lucrative. Hollywood, in its infinite generosity, wants to accelerate the release of its material to the public in nonphysical form—that is, online, cable, satellite, and IPTV (Internet Protocol television)—but is paranoid that recipients might make and distribute perfect digital copies. Therefore, content-rights owners want to be able to embed selectable-output-control bits in the digital streams, downscaling or completely disabling video outputs deemed unacceptable or even remotely shutting off receivers!

Although there is *some* justification to content-rights owners' concerns regarding in-the-clear digital bit streams, these concerns are overblown. Snagging an uncompressed HDMI (high-definition-multimedia-interface) or DisplayPort bit stream traversing the link between a set-top box and a TV, for example, would require both tremendous capture-hardware speed and tremendous capture-storage capacity.

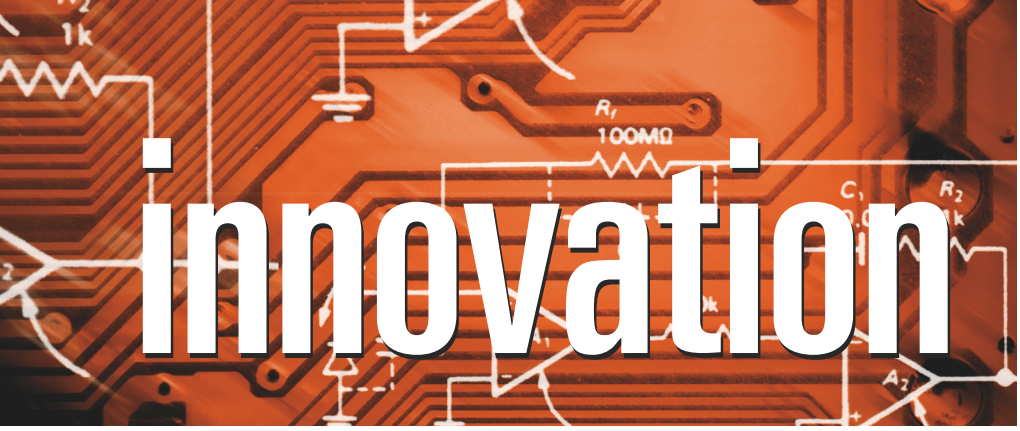
The so-called analog hole is even more laughable. Analog-tethered material has to go through iterative and inevitably quality-degrading digital-to-analog and analog-to-digital conversions as part of any duplication process. And the analog-centric copying must occur at real-time speeds; go faster than that, and you end up with all sorts of aliasing artifacts. At two hours to make a single copy of a two-hour Hollywood blockbuster, the economics don't pan out for a would-be pirate.

My big concern is that, once Hollywood gains the selectable-output-control sword it's seeking, it will broadly flex its resultant content-restriction muscle far beyond the before-DVD-release window it's currently using as justification for the scheme.

All I see selectable output control doing is increasing system cost and, by also increasing consumer frustration, hampering hardware and software sales along with expansion of the overall content ecosystem. If you agree, then I urge you to let your government representatives and FCC members hear your opinions in a loud, clear, and repeated fashion. **EDN**

Contact me at bdipert@edn.com.

Go to www.edn.com/090108eda for a more in-depth discussion of this topic.



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PRESIDENT, BOSTON DIVISION, REED BUSINESS INFORMATION
Mark Finkelstein, mark.finkelstein@reedbusiness.com
1-781-734-8431

PUBLISHER, *EDN* WORLDWIDE
Russell E Pratt, 1-781-734-8417;
rpratt@reedbusiness.com

ASSOCIATE PUBLISHER, *EDN* WORLDWIDE
Judy Hayes, 1-408-421-3799;
judy.hayes@reedbusiness.com

VICE PRESIDENT, EDITORIAL DIRECTOR
Karen Field, 1-781-734-8188;
kfield@reedbusiness.com

EDITOR-IN-CHIEF, *EDN* WORLDWIDE
Rick Nelson, 1-781-734-8418;
rnelson@reedbusiness.com

EXECUTIVE EDITOR
Ron Wilson, 1-408-345-4427;
ronald.wilson@reedbusiness.com

MANAGING EDITOR
Amy Norcross
1-781-734-8436; fax: 1-720-356-9161;
amy.norcross@reedbusiness.com
Contact for contributed technical articles

EDITOR-IN-CHIEF, EDN.COM
Matthew Miller
1-781-734-8446; fax: 1-303-265-3017;
mdmiller@reedbusiness.com

SENIOR ART DIRECTOR
Mike O'Leary
1-781-734-8307; fax: 1-303-265-3021;
moleary@reedbusiness.com

ANALOG
Paul Rako, Technical Editor
1-408-745-1994; paul.rako@edn.com

EMBEDDED SYSTEMS
Warren Webb, Technical Editor
1-858-513-3713; fax: 1-858-486-3646;
wwebb@edn.com

MASS STORAGE, MULTIMEDIA, PCs, AND PERIPHERALS
Brian Dipert, Senior Technical Editor
1-916-760-0159; fax: 1-303-265-3187;
bdipert@edn.com

MICROPROCESSORS, DSPs, AND TOOLS
Robert Cravotta, Technical Editor
1-661-296-5096; fax: 1-303-265-3116;
rcravotta@edn.com

NEWS
Suzanne Deffree, Managing Editor
1-631-266-3433; sdeffree@reedbusiness.com

POWER SOURCES, ONLINE INITIATIVES
Margery Conner, Technical Editor
1-805-461-8242; fax: 1-805-461-9640;
mconner@reedbusiness.com

DESIGN IDEAS EDITOR
Martin Rowe
edndesignideas@reedbusiness.com

SENIOR ASSOCIATE EDITOR
Frances T Granville, 1-781-734-8439;
fax: 1-303-265-3131;
f.granville@reedbusiness.com

ASSOCIATE EDITOR
Maura Hadro Butler, 1-617-276-6523;
mbutler@reedbusiness.com

EDITORIAL/WEB PRODUCTION
Diane Malone, Manager
1-781-734-8445; fax: 1-303-265-3024
Steve Mahoney, Production/Editorial Coordinator
1-781-734-8442; fax: 1-303-265-3198
Melissa Annand, Newsletter/Editorial Coordinator
1-781-734-8443; fax: 1-303-265-3279
Adam Odoardi, Prepress Manager
1-781-734-8325; fax: 1-303-265-3042

CONTRIBUTING TECHNICAL EDITORS
Dan Strassberg, strassbergedn@att.net
Nicholas Cravotta, editor@nicholascravotta.com

COLUMNISTS
Howard Johnson, PhD; Bonnie Baker;
Joshua Israelsohn; Pallab Chatterjee

PRODUCTION
Dorothy Buchholz, Group Production Director
1-781-734-8329
Kelly Jones, Production Manager
1-781-734-8328; fax: 1-303-265-3164
Linda Lepordo, Production Manager
1-781-734-8332; fax: 1-303-265-3015

EDN EUROPE
Graham Prophet, Editor, Reed Publishing
The Quadrant, Sutton, Surrey SM2 5AS
+44 118 935 1650; fax: +44 118 935 1670;
gprophet@reedbusiness.com

EDN ASIA
Susie Newham, Managing Director
susie.newham@rbi-asia.com
Kirtimaya Varma, Editor-in-Chief
kirti.varma@rbi-asia.com

EDN CHINA
William Zhang, Publisher and Editorial Director
wmzhang@idg-rbi.com.cn
John Mu, Executive Editor
johnmu@idg-rbi.com.cn

EDN JAPAN
Katsuya Watanabe, Publisher
k.watanabe@reedbusiness.jp
Ken Amemoto, Editor-in-Chief
amemoto@reedbusiness.jp

EDN. 225 Wyman St, Waltham, MA 02451. **www.edn.com**. Phone 1-781-734-8000. **Address changes or subscription inquiries:** phone 1-800-446-6551; fax 1-303-470-4280; subsmail@reedbusiness.com. For a free subscription, go to **www.getfreemag.com/edn**. Reed Business Information, 8878 S Barrons Blvd, Highlands Ranch, CO 80129-2345. Include your mailing label.

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DSO-based software analyzes 20-GHz-bandwidth RF signals

Tektronix has announced SignalVu vector-signal-analysis software, which enables engineers to use the company's DPO7000 and DPO/DSA70000 DSOs (digital-storage oscilloscopes) to easily characterize and validate wideband and microwave spectral events. The product follows a key trend in today's communications and radar systems: the need for increased information bandwidth and accurate phase and magnitude characterization of wideband signals. SignalVu combines the signal-analysis engine of the manufacturer's RSA6100A real-time spectrum analyzer with the scopes' powerful triggering, enabling designers to evaluate complex signals having bandwidth as great as 20 GHz without the need for an external downconverter.

The single integrated scope-based package performs the functions of a vector-signal analyzer and a spectrum analyzer and provides access to the scope's Pinpoint trigger capabilities. The result is an RF-test unit whose price is lower than that of alternatives for work on wideband-RF components, system design and integration, performance verification, and spectrum management.

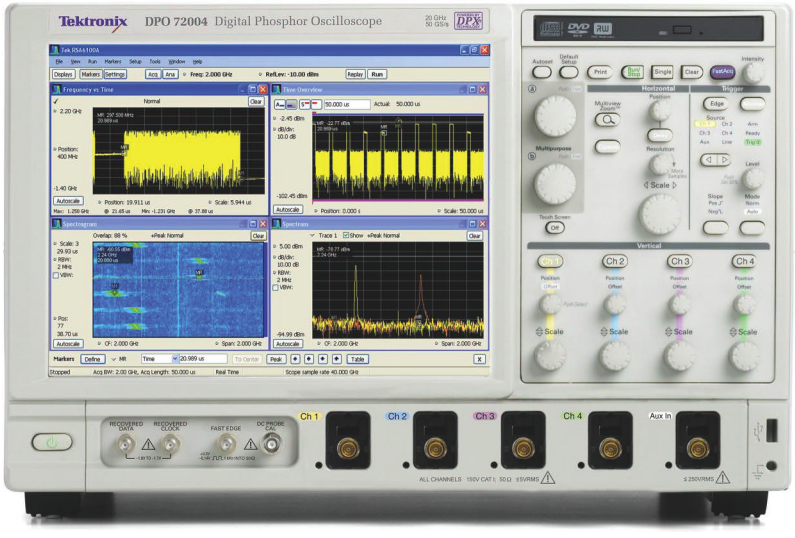
SignalVu controls all scope acquisition parameters, such as record length, vertical scaling, and sample rate. The only limit on acquisitions is the scope's memory depth. The scopes' Pinpoint trigger system allows selection of virtually all trigger types for both A and B trigger events whether they are transition, state, time, or logic-qualified triggers. Once it triggers the events, SignalVu processes the acquisition for analysis in multiple domains, allowing multiple measurements without the need to recapture the data. The scope's deep memory records all signals within the acquisition bandwidth. SignalVu lets you simultaneously capture four channels for analysis.

You can order SignalVu on all DPO7000 and DPO/DSA70000 series scopes. The basic package is SignalVu Essentials, which provides 11 core measurement and analysis capabilities. US suggested pricing starts at $3490 for scope models in the DPO7000 Series and $4990 for those in the DPO/DSA70000 Series. Options include pulse measurement and modulation analysis.

For an expanded write-up on this product and its capabilities, go to www.edn.com/article/CA6608091.

–by Dan Strassberg

▷**Tektronix Inc**, www.tektronix.com.



SignalVu software installs in several of the manufacturer's high-performance scopes and enables them to perform multiple simultaneous analyses of RF signals with bandwidths as high as 20 GHz. Such analyses previously required multiple instruments.

FEEDBACK LOOP

"Stevie Wonder said it best: When you believe in things that you don't understand, you will suffer."

—Engineer and *EDN* reader Carl Spearow, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6615600. Add your comments.

Precise monitoring maximizes HEV-lithium-ion-battery performance

Linear Technology has been working closely with a major HEV (hybrid-electric-vehicle) manufacturer in developing the LTC6802 high-voltage, precision battery-stack-monitor chip. The vehicle builder is making the transition from nickel-metal-hydride to lithium-ion-battery technology, which, according to Linear, is rapidly overcoming the shortcomings that have prevented its use in HEVs. For example, changes in the cell chemistry eliminate the thermal-runaway problem, and new cell designs remove any ignition points that can lead to fires in the event of electrical failure or mechanical damage.

The need for precision cell-by-cell monitoring of battery voltage remains, however, and, in an HEV—or a purely electric—vehicle, battery stacks may deliver hundreds of volts: Linear mentions arrays of 96 cells. The lithium-ion cells have a flat discharge curve, and, to maximize their life, you ideally use 30 to 70%—or, in some cases, 20 to 90%—of their total capacity. Therefore, you need to measure to millivolt precision to assess the state of charge of each cell; the so-called gas-gauging approach, which consists of counting charge into and out of each cell, is not viable. The 6802 therefore measures the voltage of as many as 12 cells in a series-connected stack. You can stack multiple 6802s in series for larger battery packs with a voltage as high as 1000V; they have a level-shifting interface that permits such a connection without requiring optocouplers or isolators. With a precision-trimmed internal 10-ppm/°C voltage reference, the chip is accurate to 0.25% over −40 to +85°C. It has built-in diagnostics and fault detection, communicating through an SPI (serial-peripheral interface), and Linear has qualified it to AEC (Automotive Electronics Council)-Q100 for automotive use.

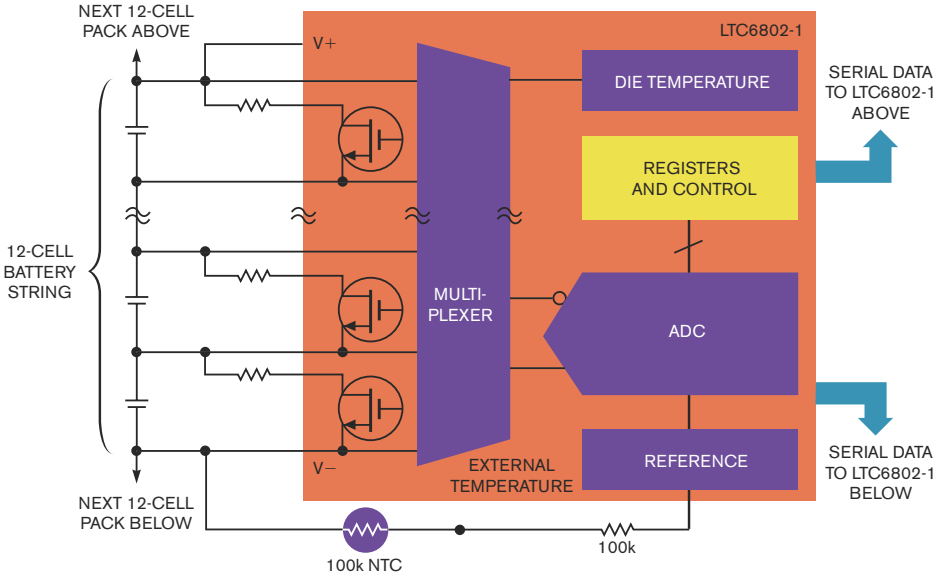
> The chip must work in an electrically noisy environment, with acceleration and regenerative-braking currents of hundreds of amperes.

The chip must work in an electrically noisy environment, with acceleration and regenerative-braking currents of hundreds of amperes. Linear designed it using a delta-sigma ADC with integral FIR (finite-impulse-response) filtering to cope with such a signal environment. It completes measurement of all the cells in a stack in 13 msec.

The chip also implements cell balancing by resistively discharging cells that are at higher voltages than neighboring cells by a current of as much as 50 mA. You might use the 6802 in applications such as robotics, portable medical equipment, high-power electric tools, or uninterruptible-power supplies, as well as in vehicles. It is available for sampling now and costs $9.95 (1000).

–by Graham Prophet

▷**Linear Technology**, www.linear.com.



The LTC6802 battery-stack-monitor chip measures the voltage of as many as 12 cells in a series-connected stack. You can stack multiple 6802s in series for larger battery packs with a voltage as high as 1000V.

DILBERT By Scott Adams

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ANALOG DEVICES

FPGA-based PXI modules improve test-system-I/O performance

NI (National Instruments) has introduced a new generation of open, FPGA (field-programmable-gate-array)-based PXI (peripheral-component-interconnect-extensions-for-instrumentation) modules. The company calls the FlexRIO (real-time-input/output) family the industry's first commercial, off-the-shelf product line to combine high-speed, instrument-class I/O with flexible LabView FPGA technology. The new products enable engineers to add custom signal-processing algorithms to PXI-based FPGA hardware. Interchangeable adapter modules directly interface FPGAs to instrument-class I/O or allow the creation of custom front-end hardware to meet application requirements. With these capabilities, you can use techniques such as inline processing, hardware-in-the-loop simulation, and protocol-aware test as you design and test complex electronic devices.

"LabView FPGA technology will continue to transform instrumentation and extend graphical-system design by providing software programmability at the hardware level," says James Truchard, PhD, the company's president, chief executive officer, and co-founder. "FlexRIO lets engineers use commercial, off-the-shelf hardware to implement applications that previously required costly custom devices with time-consuming development schedules."

FlexRIO FPGA-based hardware modules feature Xilinx (www.xilinx.com) Virtex-5 high-performance FPGAs, which you can program using the LabView FPGA-software module. Previously, according to NI, only hardware engineers who had extensive knowledge of digital design could use FPGA technology. Now, however, LabView FPGA's intuitive graphical programming makes the technology available to all engineers and provides direct access to the digital pins of the FlexRIO FPGA modules, including units that provide 66 differential or 132 single-ended lines. Each differential pair handles data rates as high as 1 Gbps, whereas each single-ended line handles rates to 400 Mbps. The modules, which offer deep onboard memory, also accommodate external clocks.

Each FlexRIO configuration comprises a pair of hardware components—an adapter module (left), which defines the system's I/O capabilities, and a PXI FPGA module (right).

Each FlexRIO configuration comprises a pair of hardware components—an adapter module, which defines the system's I/O capabilities, and a PXI FPGA module. The NI 6581 high-speed digital-I/O adapter works well for algorithmic pattern generation and protocol-aware tests. It delivers 100 MHz of digital I/O, or 200 Mbps at the double data rate, through 54 single-ended channels with selectable voltage levels of 1.8, 2.5, and 5V-compatible 3.3V. The manufacturer has also worked with Averna (www.averna.com) to create a plug-and-play IEEE 1394b adapter and expects third parties to offer many additional adapters.

You can also design your own custom adapters with converters, buffers, clocks, and connectors that suit your application. To help you develop your own modules, the FlexRIO adapter-module-development kit features full documentation of electrical- and mechanical-design details, including CAD (computer-aided-design) files and PCB (printed-circuit-board) outlines and various adapter-module enclosures.

US prices for the NI 6581 high-speed digital-adapter module begin at $999. NI PXI-795xR FlexRIO FPGA module prices begin at $2999. Prices for the NI FlexRIO adapter-module-development kit begin at $4999.

–by Dan Strassberg

▷**National Instruments**, www.ni.com/flexrio.

01.08.09

RF-COMMUNICATIONS SOFTWARE SPANS SIGNAL GENERATION AND ANALYSIS

Keithley Instruments has expanded its free SignalMeister software platform to include RF-signal analysis and generation. It controls generation and analysis of both SISO (single-input/single-output) and MIMO (multiple-input/multiple-output) signals in the same environment using the same block-diagram-based graphical user interface. It supports the latest wireless MIMO protocol standards–WiMax (worldwide interoperability for microwave access) Wave 2 and 802.11n WLAN (wireless local-area network)–and provides additional complex functions, such as WLAN-channel modeling, beam forming, simulation studies, IQ (in-phase/quadrature) operations, and full utilities for data import and export.

SignalMeister software operates with Keithley's series 2800 VSAs (vector-signal analyzers) and series 2900 VSGs (vector-signal generators) through these instruments' LXI interface for simplified test-system setup, start-up, and multi-instrument synchronization for MIMO-test systems. Users can set up test systems with one channel to 8×8 MIMO channels. The platform also includes I and Q impairments, such as frequency shift and noise.

–by Graham Prophet

▶**Keithley Instruments, www.keithley.com/signal.**

RAQs

Rarely Asked Questions

Strange stories from the call logs of Analog Devices

What's in Your Toolbox?

Q. Do you prefer power tools or hand tools for solving problems?

A. I prefer hand tools for small to medium sized jobs and power tools for large jobs.

Every day we use "tools" to get things done. In the engineering world, our toolbox is full of all sorts of things: spreadsheets, circuit and mechanical simulation programs, number crunching software (power tools) —you name it, we've got it. The latest and greatest, new-fangled tools aren't always the best options for solving problems, however. "The right tool for the job" can make all the difference in the world.

There's nothing like using a finely crafted and tuned tool for tackling a difficult or delicate job. Using one of my vintage Stanley planes in the shop is always a pleasure, and I'm constantly rewarded by its performance … but I digress.

A true test of a tool's usefulness is how often you reach for it, and how comfortable you are with it. At the office, I have an entire arsenal of tools to solve the day-to-day problems we encounter in applications, but my two favorites are Thévenin's theorem and superposition (hand tools). On a white board or piece of paper, these tools enable me to rapidly simplify and solve complex circuit problems. They particularly lend themselves to op amp and differential amplifier applications.

You might laugh that someone would opt to write out a problem by hand, given all the automation and computing power available today. By the time you open a simulation program, enter the schematic, and run the simulation, I can usually have the answer using good old Thévenin's theorem or superposition.

Thévenin's theorem, you may recall, allows you to replace a linear network with an equivalent open circuit voltage, V_{Th}, and an equivalent series resistor, R_{Th}. To determine R_{Th}, all independent voltage sources are shorted, while independent current sources are open circuited. Superposition addresses linear networks with multiple independent sources. The contribution from each source is calculated individually, while the other voltage and current sources are set to zero. The individual results are then summed to determine the output. The combination of these two tools is extremely powerful.

So, next time you find yourself reaching for a "power tool," stop and think for a moment. Perhaps a "hand tool" might be a better choice. What's your favorite work or hobby tool? Send me an email at (john.ardizzoni@analog.com), and I'll mention two or three of you and your favorite tools in my next RAQ.

To learn more about Design Tools

http://designnews.hotims.com/23090-101

Contributing Writer John Ardizzoni is an Application Engineer at Analog Devices in the High Speed Linear group. John joined Analog Devices in 2002, he received his BSEE from Merrimack College in N. Andover, MA and has over 29 years experience in the electronics industry.

Have a question involving a perplexing or unusual analog problem? Submit your question to:

raq@reedbusiness.com

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Portable MSO line features $4300, 100-MHz-bandwidth unit

Tektronix's new MSO-2000 MSO (mixed-signal-oscilloscope) and DPO2000 DPO (digital-phosphor-oscilloscope) series offer tools to simplify debugging of mixed-signal designs. These tools include Wave Inspector search-and-navigation capabilities, automatic decoding of serial data buses, and FilterVu variable-lowpass filters to reduce unwanted noise superimposed on signals. With bandwidths as great as 200 MHz, the new series complement the MSO4000, DPO4000, and DPO3000 families to provide advanced features for engineers who work on embedded-system designs. Such designs have replaced parallel buses with serial-data buses, such as I^2C (inter-integrated circuit), SPI (serial-peripheral interface), RS-232, CAN (controller-area network), and LIN (local-interconnect network).

The MSO2000 sports Tek scopes' familiar front-panel layout.

On a serial bus, one signal can combine address, control, data, and clock information, and that complexity presents significant debugging challenges. The entry-level MSO2000 and DPO2000 series address these problems with integrated serial-data-triggering, protocol-decoding, and analysis capabilities. The MSO2000 also time-correlates as many as four analog and 16 digital signals.

Each series comprises three models that have two or four 100- or 200-MHz-bandwidth analog channels. Other features include serial triggering; protocol decoding; USB (Universal Serial Bus) plug-and-play connectivity; a bright, 7-in. wide-screen display; and a three-year warranty. All models capture 1 million-point records on each channel and acquire 1G sample/sec on all analog channels, ensuring that all signals within the analog bandwidth undergo sampling at least five times per cycle. To aid discovery of elusive transients, all MSO2000- and DPO2000-series units capture 5000 analog waveforms/sec.

The new FilterVu variable-lowpass filter blocks unwanted noise without reducing the bandwidth of the signals you are investigating. The two series simultaneously display the filtered waveform and high-frequency details that contain frequencies as high as the scope's full analog bandwidth. On all analog and digital channels, both series include the Wave Inspector search engine, a set of easy-to-use tools that makes short work of finding events of interest in long records. Wave Inspector can also automatically search through an acquisition, mark all occurrences of a user-specified event, and then navigate effortlessly among the marks.

All models include a USB-host port on the front panel and a USB-device port on the rear. The front USB port supports a flash drive. The rear port is compatible with the test-and-measurement version of USB, which enables communication and control through a PC. The rear port is also PictBridge-certified for printing to PictBridge-certified printers. US list prices range from $2580 to $5150. MSO models include a P6316 digital probe. The 100-MHz-bandwidth, four-channel MSO2014 costs $4300.

–by Dan Strassberg

▷**Tektronix Inc**, www.tektronix.com/scopes.

EDN BLOG

PRACTICAL CHIP DESIGN

Economists, mathematics, and where the semiconductor industry is headed

A snide person might observe that, if circuit designers were equipped with the same formidable mathematical skills as economists, we would all be using single-ended triode amplifiers that oscillated when we turned the gain up. (As it is, only the very rich get to use these, but that's another rant altogether.)

In my local newspaper this morning was an article reporting that the housing market was in "a tailspin" with no hope in sight. I suppose that the implication was that, if you don't own your home outright, you'd just as well pack up and move to an apartment now and waste no more money on mortgage payments.

Unfortunately for the reporter's premise, he or she published along with the article a graph of housing prices versus time. It showed a slightly damped cosine wave—the sort of time-domain response you would expect if you hit a slightly underdamped system with a downward step function.

The thing that caught my attention was that the inflection point on the cosine wave occurred in about April. According to the data—as opposed to the text—the rate of descent has actually been decreasing for almost a full quarter. That suggests we could see a bottom to the housing-price decline, at least in terms of national averages, sometime in the third or early fourth quarter. This minor detail was completely lost on the author of the news story. It made me once again wish that economists, reporters, and others who directly influence public sentiment about the economy were required to pass at least one course in linear systems before they were allowed access to a keyboard.

–by Ron Wilson

▶www.edn.com/practicalchipdesign.

▶For the full post, go to www.edn.com/090108ba.

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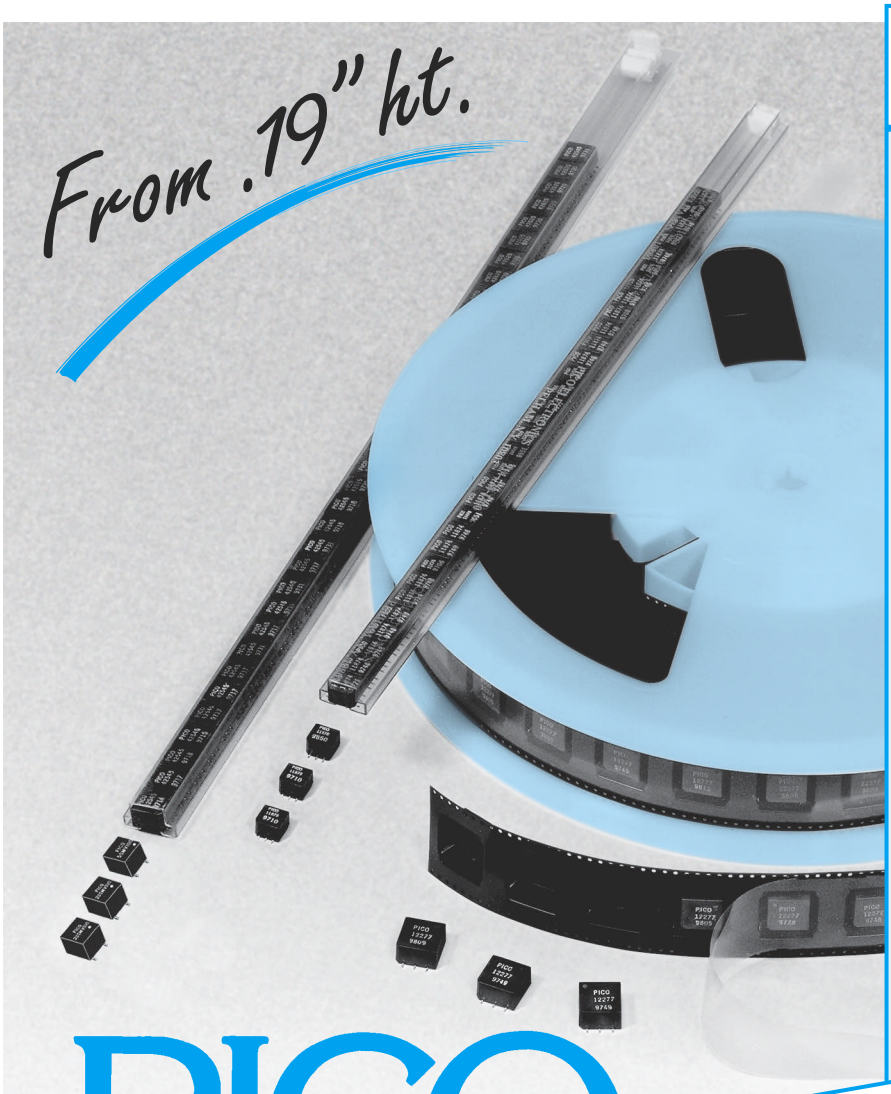

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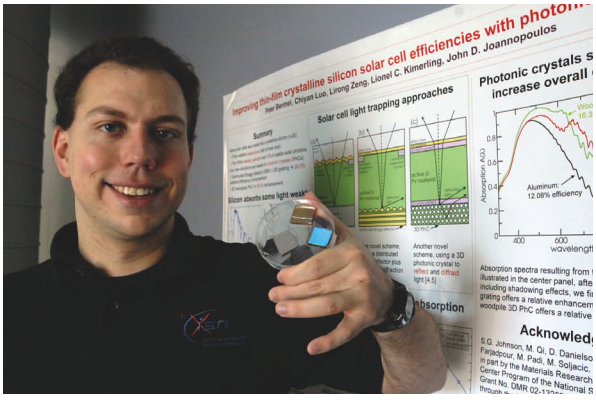
RESEARCH UPDATE

BY MATTHEW MILLER

MIT researchers claim 50% increase in solar-cell output



MIT postdoctoral student Peter Bermel displays examples of the materials his research team employs to obtain a claimed 50% increase in solar-cell efficiency (courtesy Donna Coveney).

A team of physicists and engineers at MIT (Massachusetts Institute of Technology) claims that sandwiching a solar cell between an antireflective coating on the front and a combination of reflective coatings and a diffraction grating on the back can increase the cell's output by as much as 50% for a 2-micron-thick cell.

The aim of the coatings and grating is to keep photons of incoming light bouncing around longer within the thin silicon cell, thereby increasing the likelihood that they will deposit their energy and produce a current rather than just escaping back out into the surrounding air. The team used simulation to experiment with the spacing of the diffraction grating's lines, the number and thickness of reflective coatings, and the thickness of the silicon before verifying the findings in the lab.

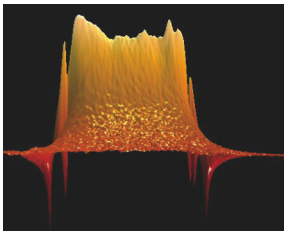
Because the work applies to extremely thin silicon cells, the researchers cite reduced silicon cost as another benefit of their approach, stating that their thin films use about 1% as much silicon as conventional solar cells.

▷**Massachusetts Institute of Technology**, www.mit.edu.

Tests resolve tension over silicon strain

In work that should help silicon-device makers optimize materials and processes, scientists at the NIST (National Institute of Standards and Technology) have demonstrated the ability to measure stress in regions of a semiconductor device as small as 10 nm in diameter.

The testing also helps to explain a longstanding discrepancy between two methods of measuring such strain: CRM (confocal-Raman microscopy), which measures frequency shifts in photons after they interact with atomic bonds in the crystal, and EBSD (electron-backscattered diffusion), which analyzes the patterns of electrons bouncing back from crystal planes. Using refined forms of both types of instruments, the NIST researchers discovered the reason for the differing measurements: Whereas EBSD samples only the top 20 or 30 nm of a material, the photons in CRM penetrate 1 micron or more. By varying the wavelength and focus of a CRM system so that it measured the same region as EBSD, the researchers obtained results that agreed closely.



A CRM system presents the magnitude of stress induced in a silicon crystal by indentation with a 20-micron-long wedge.

By in essence calibrating the two types of strain measurements, the work should help device makers control not only unwanted stress, which can, for example, shift the output color and reduce the lifetime of LEDs, but also the desirable stress that chip makers deliberately create to enhance transistor speed.

▷**NIST**, www.nist.gov.

FUTURE NONVOLATILE MEMORIES MAY HAVE CARBON FOOTPRINTS

01.08.09

A Rice University team has proposed that a strip of graphene 10 atoms thick could serve as the basic storage element in a new form of memory. With individual bits smaller than 10 nm, the memory's capacity would improve upon today's state-of-the-art flash memory by a factor of five when comparing 2-D arrays. Moreover, two terminals rather than three would control the new switches, making it practical to further increase density by stacking sheets of the material into 3-D arrays, according to the researchers.

Graphene sports an on/off power ratio of 1 million-to-one, the team states, enabling much larger arrays than other nonvolatile technologies, such as phase-change memory. Finally, the researchers say they have tested the technology over 20,000 cycles with no degradation and found it to be immune to temperature over −75 to +200°C.

In separate work, researchers at the United Kingdom's University of Nottingham are working on a form of memory that would employ as its basic element a carbon nanotube nested within another slightly larger carbon nanotube. Application of power would force the inner tube to telescope into and out of the larger one, alternately bringing it into and out of contact with an electrode. In an unpowered state, the van der Waals force would keep each inner tube in place to preserve the stored data.

▶Rice University, www.rice.edu.

▶University of Nottingham, www.nottingham.ac.uk.

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BY HOWARD JOHNSON, PhD

Differential transitions

Figure 1 depicts one corner of an FPGA package. The **figure** shows the balls on the bottom side of the FPGA as they would appear from underneath the package. You could never see this view in a real application. In this photo, portions of the PCB (printed-circuit board) appear transparent to reveal the vias plunging down to lower layers in the board.

The FPGA package contains a large number of controlled-impedance traces. Those traces connect the die to the balls on the underside of the package. The traces are laid out on a tiny BGA (ball-grid-array) substrate inside the FPGA package. The substrate incorporates multiple solid power and ground planes, much like a normal PCB.

Drawn with pink and blue highlights, a differential-signal pair exits the FPGA on two adjacent balls. The differential pair is routed on PCB Layer 1. The dielectric beneath Layer 1 is transparent, so you can see the bottom side of the two traces as they lead away from the package.

The path through the balls is a transition region. From the tiny traces inside the BGA package, the differential signal flows down through the balls to the lower world of much larger Layer 1 traces on the PCB. As your signal passes through the transition region, the differential impedance of that area depends mostly on the geometry of the two balls at the point of exit, the two traces, and their relation to the nearest underlying solid reference plane in the PCB.

The configuration in **Figure 1** is the most favorable exit strategy for a differential pair in a BGA package. The entire path is compact and symmetric with respect to the surrounding planes. With the differential-signal traces on Layer 1, no drilled holes or vias complicate the situation.

Signal transitions occur wherever your signal passes through a package body, a connector, or a pair of vias. Whatever the geometry of your design, if you keep the entire transition region smaller than the rise and fall time of the driver, you can average together the details of that geometry into a simple approximation for the transition region. That approximation is commonly represented as one short section of differential transmission line with characteristic impedance, Z_1, different from the characteristic impedance of the surrounding transmission structure, Z_0. Because you can average the properties of compact structures over their extent, you can compensate for imperfections at one point within the transition by counterbalancing imperfections at other points within the transition region.

For example, if the ball spacing is too large, driving Z_1 too high, compensate by increasing the size of the BGA solder pads, thus adding capacitance and driving Z_1 back down to the correct average value. Inserting near-by compensation to fix problems elsewhere within the transition region is the secret to successful transition design. It works only when the overall transition delay is less than about one-tenth of the signal rise or fall time.

Figure 1 The differential pair exits the BGA package on Layer 1.

If your transition delay exceeds one-tenth of the signal rise or fall time, then you must break the transition down into subsections, each small enough to satisfy the one-tenth rule, and then separately compensate the average impedance within each subsection.

To help you gauge the difficulty of transition design, **Table 1**, which is available in the online version of this column at www.edn.com/090108hj, computes the total delay of a few common transitions. In each case, the **table** shows the minimum rise/fall time for which the structure acts in a simple, lumped-element manner, and you can easily tweak it to obtain optimum performance.EDN

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.

Go to www.edn.com/090108hj and click on Feedback Loop to post a comment on this column.

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BY PALLAB CHATTERJEE, CONTRIBUTING TECHNICAL EDITOR

Physical design and architectural design

Historically, in the semiconductor-design flow, tapeout came after the last stages of the physical-design creation and verification. It was the final step before the design entered the manufacturing process, and it typically occupied less than 20% of the project-development schedule. Generally, a group other than the design team performed the tapeout and used separate design tools to construct a manufacturable view of the design. This division of labor no longer holds true.

Most of today's big digital ICs are actually SOCs (systems on chips). As a result, the engineering-design team has to stay involved through both the block design and the physical design. The shift in physical-design tools to incorporating gate and sizing changes you base on physical-synthesis and -optimization tools now requires the involvement of engineering-design personnel through tapeout, as well. Issues that are now part of the physical-design flow include gate sizing, logic changes and optimization, buffer insertion, split-path creation, signal integrity and shielding, and IR-drop analysis. The analysis of these issues requires both the physical-design team and the block-design team.

The proliferation of deep-submicron processes has also led to an expanded tapeout scope, which now encompasses architectural design. Tapeout must address design trade-offs, such as power, I/O structures, memory structures, display interfaces, and programmability.

The power trade-offs include power-reduction methodologies, such as multithreshold CMOS, gated power, and multiple options for threshold voltage. These factors affect the overall physical-design floorplan and global routing constraints. Further, modern I/Os often require multiple power rings, also strongly impacting tapeout. These power rings usually offer minimal documentation, include complex interconnect, and require specific placement criteria.

There is a major trend in control logic toward embedding standard functions into designs.

Memory structures are typically hard macros, which means that the memory instance appears in the final chip as a placement of a complete memory block that the designers have neither edited nor modified. A third-party IP (intellectual-property) provider or a memory-compiler program—not the chip designers—creates the memory block. Such blocks are architectural elements for the tapeout team because the clustered or distributed nature of the memories and their internal organization impact the data buses and block locations in the chip.

Display interfaces are relatively new functions that both impact the tapeout flow and have architectural and block-design aspects. Historically, chips used private display interfaces connected to discrete LEDs, simple LED/LCD panels with segments and icons, or custom icon displays you could toggle that basically were printed versions of standard displays. But software configures and drives most modern displays, and the displays connect to the SOC through a standards-based interface. As a result, the timing of these interface blocks and the clustering of the I/Os for these blocks—a display port, for example—impose guidelines on tapeout teams' plans for physical placement.

As with the displays, there is a major trend in control logic toward embedding standard functions, such as microcontrollers, into designs and using external memory to program the functions. This practice minimizes the number of critical-path circuits in the design but locks much of the physical design into fixed macros. The physical-design tools behave differently with high block granularity—lots of small cells—than they do with high block obstruction—lots of big, immovable blocks with fixed pin locations. As a result, this facet of the architectural design also directly affects the number and type of tapeout-design trade-offs an SOC requires. EDN

Contact me at pallabc@siliconmap.net.

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VOL. 3

CONNECTIVITY

A FASTER-TO-MARKET STORY

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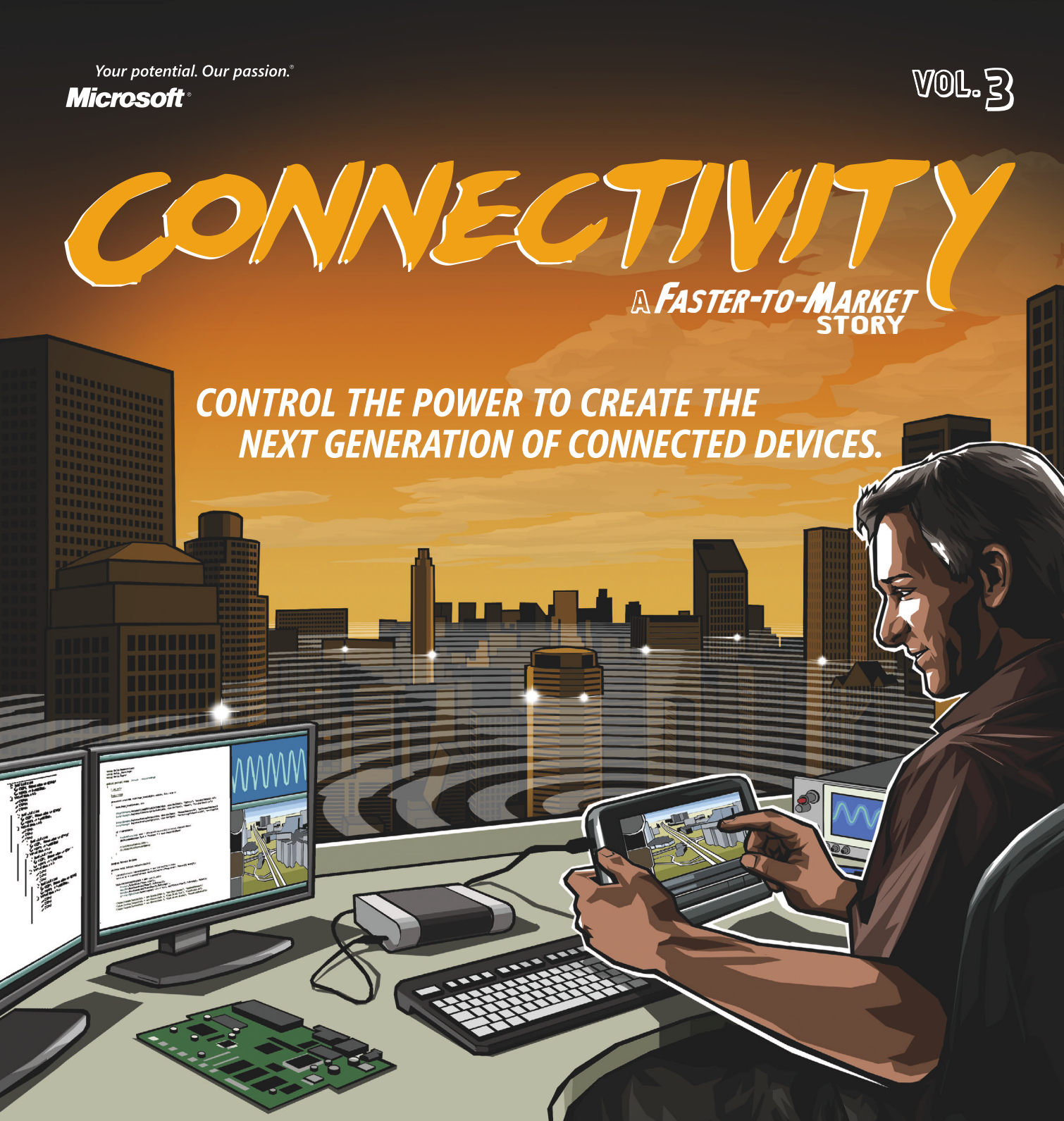

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DIODE-TURN-ON-TIME-INDUCED FAILURES IN SWITCHING REGULATORS

NEVER HAVE SO MANY HAD SO MUCH TROUBLE WITH SO FEW TERMINALS.

BY JIM WILLIAMS AND DAVID BEEBE • LINEAR TECHNOLOGY CORP

Most circuit designers are familiar with diode dynamic characteristics, such as charge storage, voltage-dependent capacitance, and reverse recovery time. Manufacturers less commonly acknowledge and specify diode forward turn-on time. This parameter describes the time required for a diode to turn on and clamp at its forward-voltage drop. Historically, this extremely short time, measured in nanoseconds, has been so small that user and vendor alike have essentially ignored it. They rarely discuss and almost never specify it. Recently, switching-regulator clock rate and transition time have become faster, making diode-turn-on time a critical issue. The industry has mandated increased clock rates to achieve smaller magnetics; decreased transition times somewhat aid overall efficiency but are principally needed to minimize IC heat rise. At clock speeds beyond about 1 MHz, transition-time losses are the primary sources of die heating.

A potential difficulty due to diode-turn-on time is that the resultant transitory overshoot voltage across the diode, even when restricted to nanoseconds, can induce overvoltage stress, causing switching-regulator-IC failure. As such, careful testing is required to qualify a given diode for a particular application to ensure reliability. This testing, which assumes low-loss surrounding components and layout in the final application, measures turn-on overshoot voltage due to diode parasitics only. Improper associated component selection and layout will contribute additional overstress terms.

DIODE TURN-ON TIME

Figure 1 shows typical step-up and step-down voltage converters. In both cases, the assumption is that the diode clamps switch pin-voltage excursions to safe limits. In the step-up case, the switch pin's maximum allowable forward voltage defines this limit. The switch pin's maximum allowable reverse voltage sets the step-down case limit.

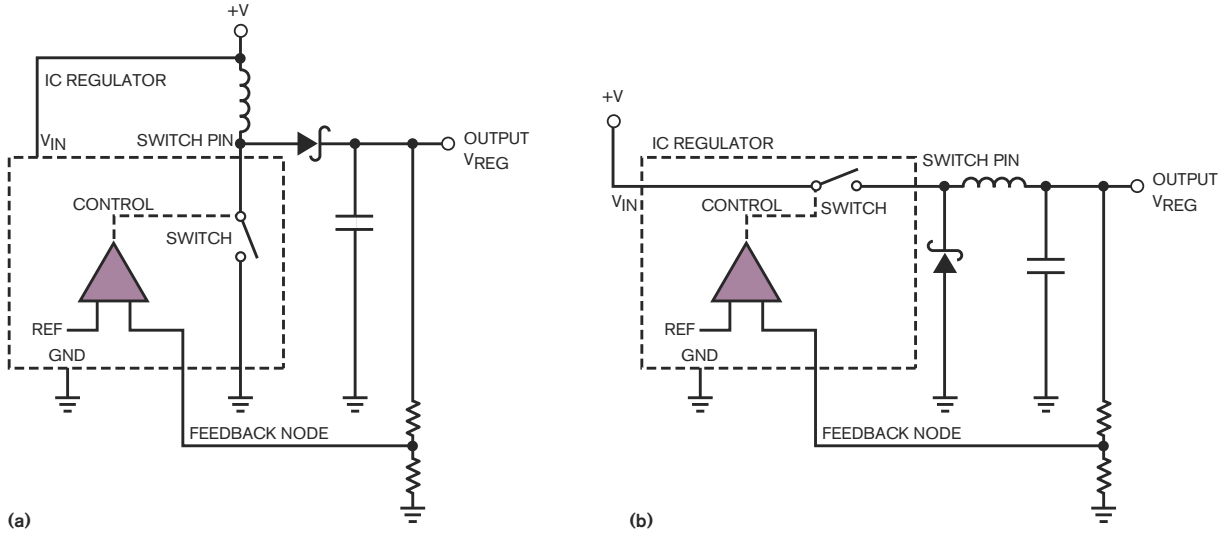


Figure 1 In both typical-voltage-step-up (a) and step-down converters (b), assume that the diode clamps the switch pin-voltage excursion to a safe limit.

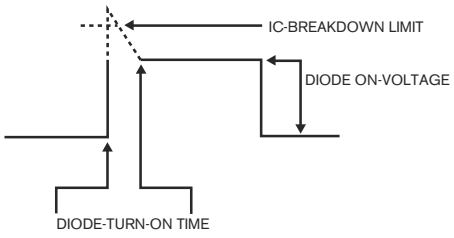


Figure 2 The diode-forward-turn-on time permits transient excursion above nominal diode clamp voltage, potentially exceeding the IC-breakdown limit.

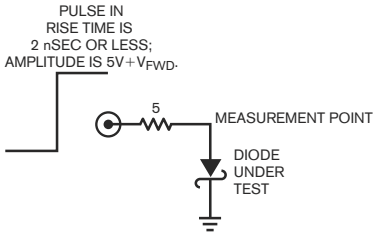


Figure 3 A conceptual method tests diode-turn-on time at 1A. The input step must have an exceptionally fast, high-fidelity transition.

Figure 2 indicates that the diode requires a finite length of time to clamp at its forward voltage. This forward-turn-on time permits transient excursions above the nominal diode-clamp voltage, potentially exceeding the IC's breakdown limit. You typically measure the turn-on time in nanoseconds, making observation difficult. A further complication is that the turn-on overshoot occurs at the amplitude extreme of a pulse waveform, precluding high-resolution amplitude measurement. You must consider these factors when designing a diode-turn-on-test method.

Figure 3 shows a conceptual method for testing diode-turn-on time. Here, the test is performed at 1A, although you could use other currents. A pulse steps 1A into the diode under test via the 5Ω resistor. You measure turn-on-time-voltage excursion directly at the diode under test. The **figure** is deceptively simple. In particular, the current step must have an exceptionally fast, high-fidelity transition, and faithful turn-on time determination requires substantial measurement bandwidth.

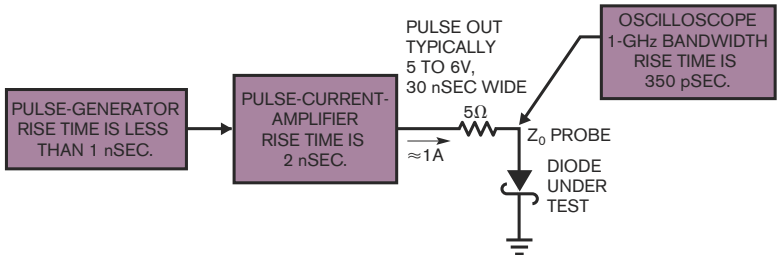


Figure 4 A detailed measurement scheme indicates necessary performance parameters for various elements.

DETAILED MEASUREMENT

Figure 4 offers a more detailed measurement scheme. The design requires a less-than-1-nsec-rise-time pulse generator; a 1A, 2-nsec-rise-time amplifier; and a 1-GHz oscilloscope. These specifications represent realistic operating conditions; you may select other currents and rise times by altering appropriate parameters (see **sidebar** "Connections, cables, attenuators, probes, and picoseconds").

The pulse amplifier necessitates careful attention to circuit configuration and layout. As **Figure 5** shows, the amplifier includes a paralleled, Darlington-driven RF-transistor-output stage. The collector-voltage adjustment, or rise-time trim, peaks Q_4 to Q_6 F_T; an in-

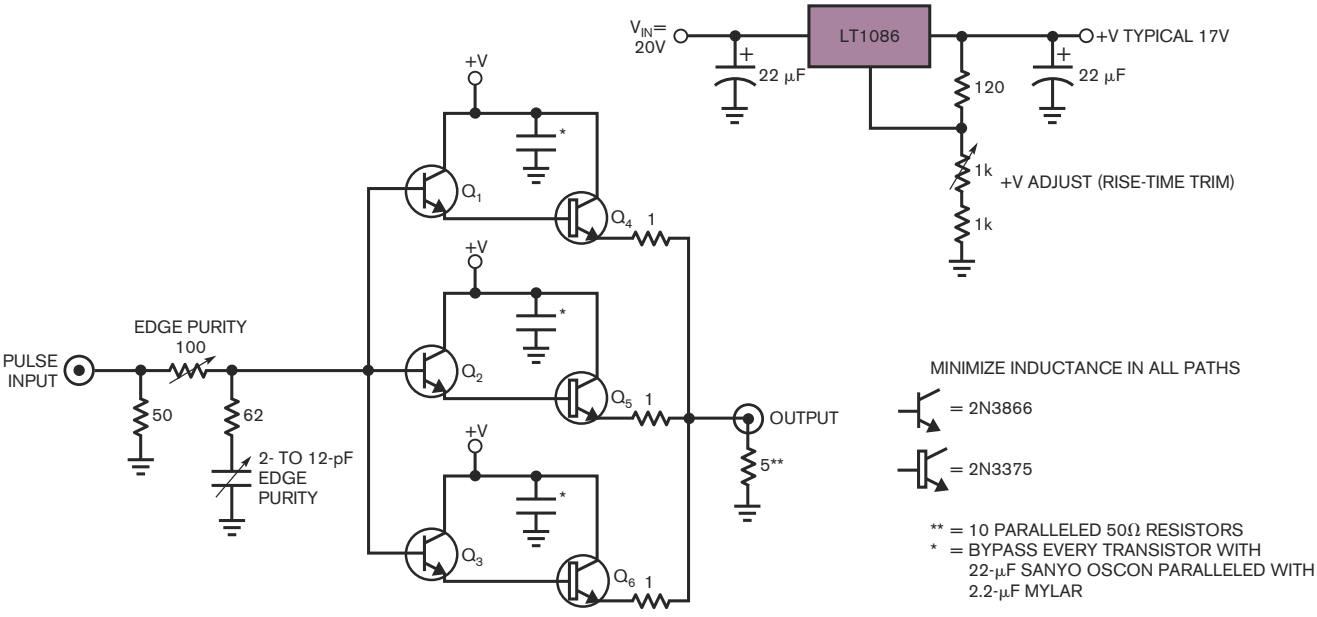


Figure 5 The pulse amplifier includes a paralleled, Darlington-driven RF-transistor-output stage. Collector-voltage adjustment, or rise-time trim, peaks Q_4 to Q_6 F_T, and the input-RC network optimizes output-pulse purity. A low-inductance layout is mandatory.

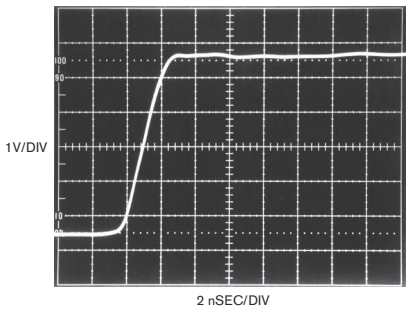


Figure 6 For a pulse-amplifier output into 5Ω, the rise time is 2 nsec with minimal pulse-top aberrations.

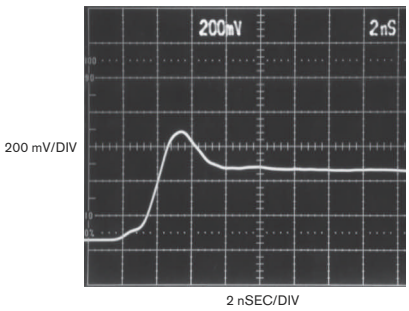


Figure 8 Diode 1 overshoots steady-state forward voltage for approximately 3.6 nsec, peaking at 200 mV.

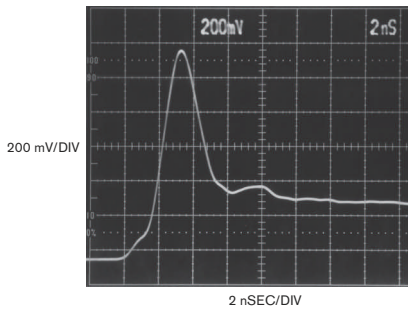


Figure 9 Diode 2 peaks at approximately 750 mV before settling in 6 nsec, more than twice the steady-state forward voltage.

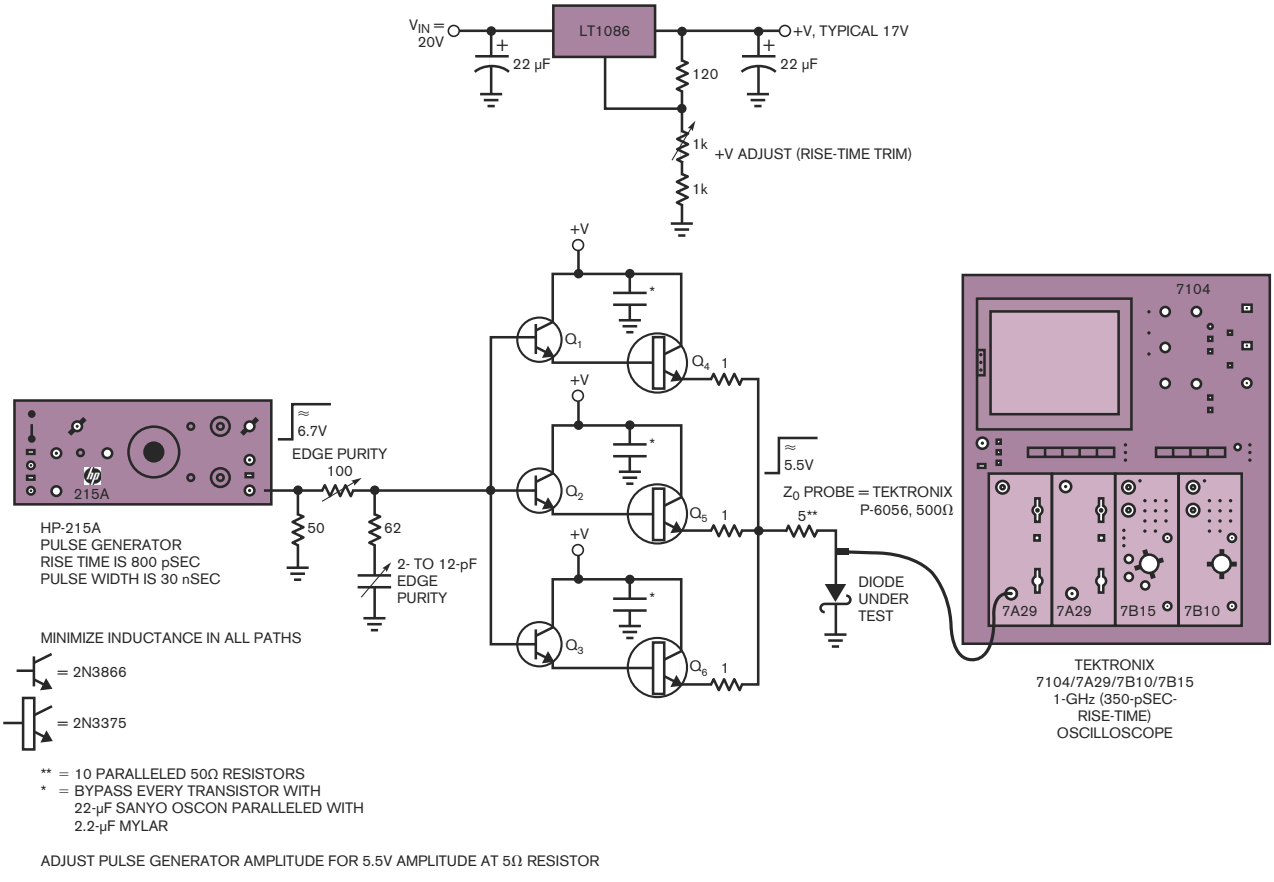


Figure 7 A complete diode-forward-turn-on-time-measurement arrangement includes a subnanosecond rise-time pulse generator, pulse amplifier, Z_0 probe, and 1-GHz oscilloscope.

put-RC network optimizes output-pulse purity by slowing the input-pulse rise time to within the amplifier passband. Paralleling allows Q_4 to Q_6 to operate at favorable individual currents, maintaining bandwidth. When you optimize the mildly interactive edge-purity and rise-time trims, **Figure 6** indicates, the amplifier produces a transcendently clean 2-nsec rise-time output pulse devoid of ringing, alien components, or post-transition excursions. Such performance makes diode-turn-on-time testing practical (see **sidebar** "Verifying rise-time-measurement integrity" in the Web version of this article at www.edn.com/090108df).

Figure 7 depicts the complete diode-forward-turn-on-time-measurement arrangement. The pulse amplifier, driven by a subnanosecond pulse generator, drives the diode under test. A Z_0 probe monitors the measurement point and feeds a 1-GHz oscilloscope.

DIODE TESTING

The measurement-test fixture, properly equipped and constructed, permits diode-turn-on-time testing with excellent time and amplitude resolution. **Figures 8** through **12** show results for five diodes from various manufacturers. **Figure 8** (Diode 1) overshoots steady-state

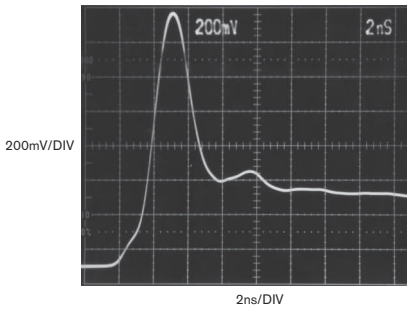


Figure 10 Diode 3 peaks at 1V above nominal 400-mV V_{FWD}, a 2.5× error.

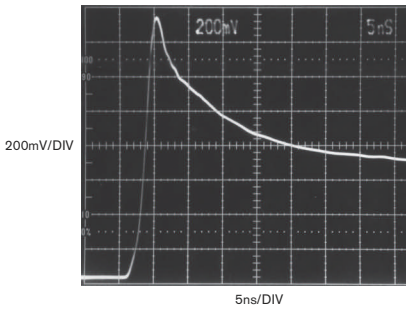


Figure 11 Diode 4 peaks at approximately 750 mV with lengthy tailing toward the V_{FWD} value. (Note the horizontal 2.5-times scale change.)

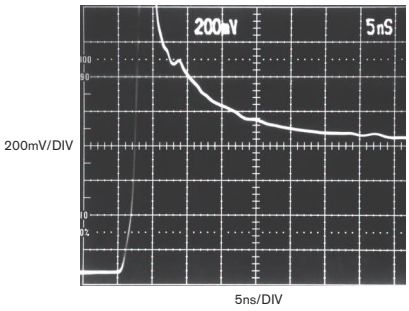


Figure 12 Diode 5 peaks offscale with extended tailing. Note the horizontal slower scale compared with figures 8 through 10.

forward voltage for 3.6 nsec, peaking at 200 mV, offering the best performance of the five. **Figures 9** through **12** show increasing turn-on amplitudes and times. In the worst cases, turn-on amplitudes exceed nominal clamp voltage by more than 1V, and turn-on times extend for tens of nanoseconds. **Figure 12** culminates this unfortunate parade with huge time and amplitude errors. Such errant excursions can and will cause IC-regulator breakdown and failure. The lesson here is clear: You must characterize and measure diode turn-on time in any given application to ensure reliability. EDN

For more sidebars related to this article and a list of references used, go to www.edn.com/090108df.

AUTHORS' BIOGRAPHIES

Jim Williams is a staff scientist at Linear Technology Corp, where he specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Laboratory at the Massachusetts Institute of Technology (Cambridge, MA). A former student at Wayne State University (Detroit), Williams enjoys sports cars, art, collecting antique scientific instruments, sculpture, and restoring old Tektronix oscilloscopes.

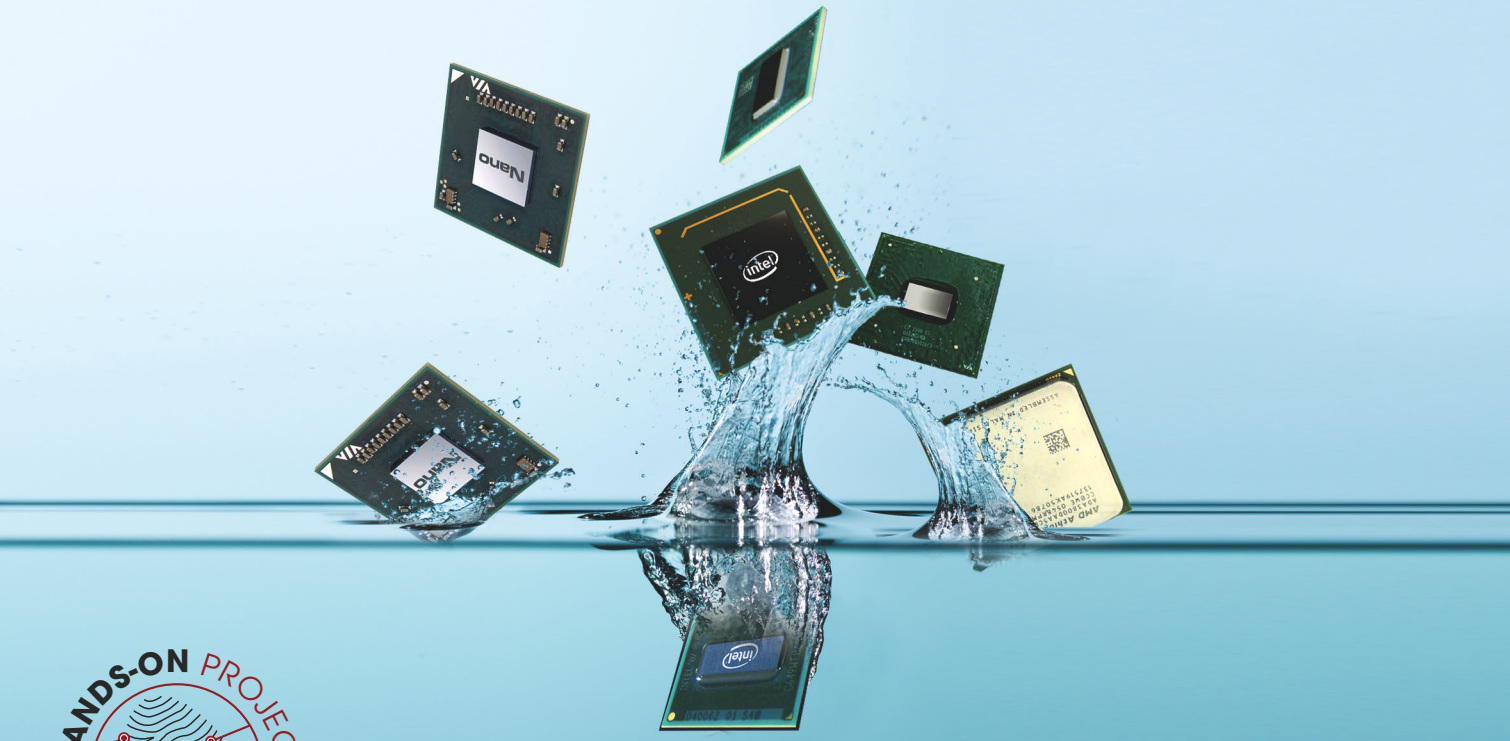
David Beebe is a product-evaluation engineer at Linear Technology Corp. He began his career in the electronics industry with Varian Associates immediately upon his discharge from the US Air Force in 1983. After 10 years with Varian's microwave-tube division, Beebe joined Linear, where he plays a key role in the development of new high-performance analog products. In his spare time, Beebe enjoys more mechanical endeavors, such as riding and racing highly modified all-terrain vehicles.

CONNECTIONS, CABLES, ADAPTERS, ATTENUATORS, PROBES, AND PICOSECONDS

You must consider rise-time signal paths of less than 1 nsec as transmission lines. Connections, cables, adapters, attenuators, and probes represent discontinuities in this transmission line, deleteriously affecting its ability to faithfully transmit the desired signal. The degree of signal corruption that a given element contributes varies with its deviation from the transmission line's nominal impedance. The practical result of such aberrations is degradation of pulse rise time, fidelity, or both. Accordingly, you should minimize the introduction of elements or connections to the signal path and use high-grade components for connections and elements.

Any form of connector, cable, attenuator, or probe must be fully specified for high-frequency use. Familiar BNC hardware becomes lossy at rise times much faster than 350 psec. SMA components are preferable for the rise times this article describes. Additionally, to minimize inductance, cable-induced mismatch, and distortion, connect the pulse-amplifier output directly to the diode under test without using cable. Avoid mixing signal-path hardware types via adapters. Adapters introduce significant parasitics, resulting in reflections, rise-time degradation, resonances, and other degrading behavior. Similarly, make oscilloscope connections directly to the instrument's 50Ω inputs, avoiding probes. If you must use probes, introduction to the signal path mandates attention to their connection mechanism and high-frequency compensation. Passive low-impedance types, commercially available in 500Ω and 5-kΩ impedances, have input capacitance of less than 1 pF (see sidebar "About low-impedance probes" in the Web version of this article at www.edn.com/090108df). You must carefully frequency-compensate any such probe before use, or measurement may be misrepresented. Inserting the probe into the signal path necessitates some form of signal pick-off, which nominally does not influence signal transmission. In practice, some amount of disturbance must be tolerated and its effect on measurement results evaluated. High-quality signal pick-offs always specify insertion loss, corruption factors, and probe-output scale factor.

Be vigilant when designing and maintaining a signal path. Skepticism, tempered by enlightenment, is a useful tool when constructing a signal path, and no amount of hope is as effective as preparation and directed experimentation.



EDN HANDS-ON PROJECT

THE PRICE OF FALLING PRICES: EVALUATING VALUE-ORIENTED x86 CPUs

ECONOMICAL MICROPROCESSORS MAY ENABLE YOU TO EASILY HIT YOUR NEXT DESIGN'S BILL-OF-MATERIALS COST TARGET, BUT WILL THEY ALSO ALLOW YOU TO ACCOMPLISH YOUR PERFORMANCE AND POWER-CONSUMPTION OBJECTIVES?

BY BRIAN DIPERT • SENIOR TECHNICAL EDITOR

It's unclear to what degree Intel anticipated the fiscal crisis now gripping the globe and therefore developed the economical Atom CPU as a means of preserving its market-share position. (The company publicly states that its primary intent with Atom was to broaden the application base for the x86 architecture.) It's also unclear what negative impact on long-term corporate revenues and profits may result from Atom's potential "cannibalization" of more lucrative Intel microprocessors. Nonetheless, *any* indication of robust sales is a rare and encouraging sign in today's economic malaise. So-called netbooks currently account for the bulk of PC-market growth, and Atom is the CPU engine powering most netbook designs, so Intel deserves kudos for pragmatism in using Atom to obsolete its own CPUs instead of allowing competitors to do so.

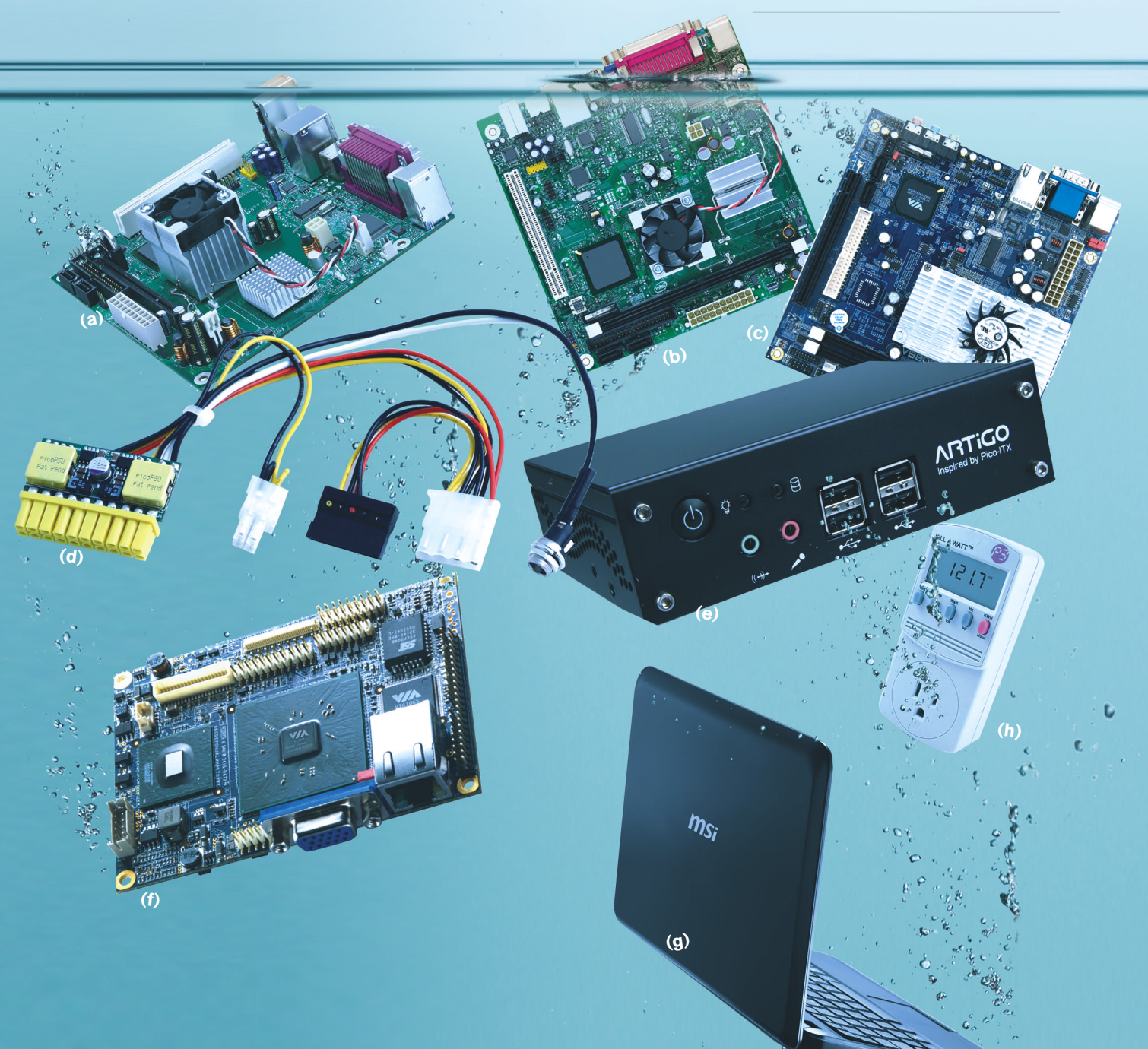


Figure 1 Intel's D945GCLF (a) and D945GCLF2 (b) mini-ITX boards provided ideal hardware test beds for, respectively, the Atom 230 and 330 CPUs, as did Via's VB8001 (c) for the company's newest Nano processor. Mini-box's compact picoPSU-90 dc/dc converter (d), in combination with a generic ac/dc 12V/5A power supply, fueled them all. Via's Artigo hobbyist kit (e) houses a C7 CPU-based pico-ITX board (f). The MSI Wind U100's (g) straightforward underclocking and overclocking capabilities were ideal for testing the Atom 270 CPU at various speeds, and P3 International's P4400 Kill A Watt (h) allowed measurement of all systems' power consumption in various operating modes.

In contrast, Via Technologies, no stranger to value-priced PCs, takes another tack. The company has long been the torchbearer of the belief that modern x86 CPUs tout capabilities that not only represent overkill for mainstream users' computing needs, but also add costs that the manufacturers must pass on to consumers. In response, Via, through its Centaur Technology subsidiary, developed the C3 and C7 microprocessor families, which Via recently augmented with the Nano CPU. The C7-to-Nano transition markedly differs from the approach that Intel took in developing Atom, however. As I noted last spring, just as Intel was stripping out-of-order execution and other superfluous features from its previous architectures, Via's Centaur subsidiary was poised to unleash the company's first three-way superscalar out-of-order architecture (**Reference 1**).

This hands-on project is the latest attempt to answer the question: Which approach—Intel's or Via Technologies'—is better for your design needs (see **sidebar** "Whither AMD?" as well as **Table 1** and **Reference 2**). Testing stand-alone CPUs is of little practical benefit: Although the CPUs act as the brains of the systems surrounding them, the capabilities and limitations of those systems also influence them (**Table 2**). And raw-CPU-speed tests wouldn't adequately represent the breadth of design requirements that contend for your attention. You must be sure to normalize performance measurements against the processor's core clock rate. This article also provides power-consumption and price data to act as additional calibration fodder.

TEST-SUITE DETAILS

A 1.6-GHz, Atom 230-based Intel D945GCLF mini-ITX board came from Ituner Networks, whose company's Minibox subsidiary makes the picoPSU-90 power supply that fueled all three mini-ITX products in this project (**Figure 1**). Its near-twin, a 1.6-GHz, Atom 330-based D945GCLF2, came from Mobile Computing Solutions by way of eBay. The two boards look identical at first glance, aside from their CPUs, which Intel intends for use with low-cost, ac-powered PCs and other x86-based systems. A closer inspection reveals telltale differences, however: The D945GCLF2 populates, through a connector module, the s-video-output solder-pad sites on both boards, and the boards' core-logic north-bridge-IC passive-heat-sink designs also differ.

The third mini-ITX board in this project is Via's 1.6-GHz VB8001 Nano platform. One key difference between it and the Intel boards relates to system memory: Whereas the Intel boards incorporate only one DIMM slot supporting DDR2-533-speed maximum-memory rates, the VB8001 includes two slots that can each handle DDR2-667 SDRAMs at full speed. I wanted to test all three boards at equivalent 2-Gbyte aggregate capacities, so I populated each of the VB8001 SDRAM connectors with a 1-Gbyte DIMM. I re-

AT A GLANCE

- Small-form-factor boards and systems proved ideal for testing the CPUs on and inside them.
- CPU performance depends on both clock rate and function.
- Keep in mind the impact of both cache and system memory on the processor cores you mate them with.
- A high-performance processor won't fill the bill unless it also achieves your design's power-consumption targets.
- Vendors have different ideas on how much price info to disclose.

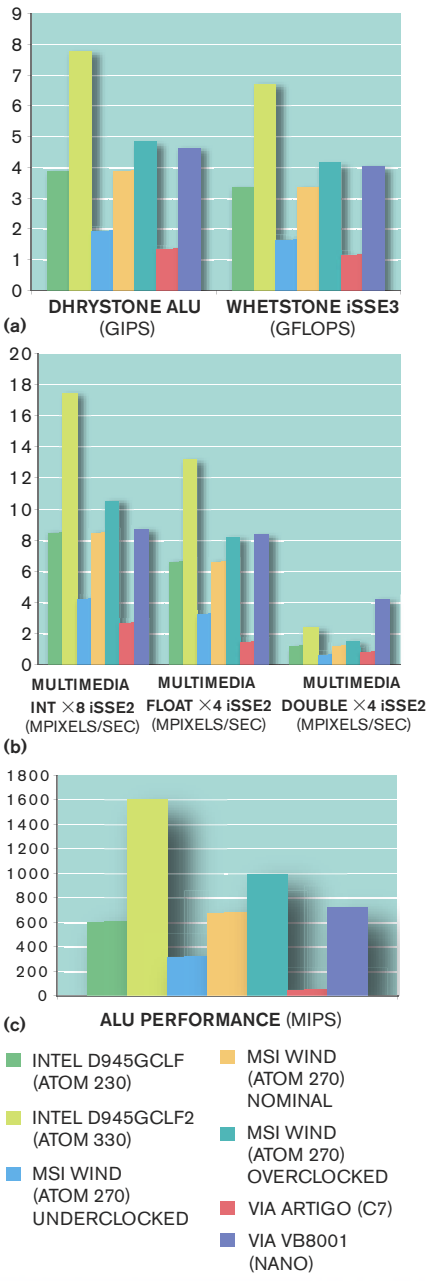


Figure 2 Generic-processor tests in the Sandra suite produced telling statistics in Processor Arithmetic (a), Processor Multimedia (b), and Power Management Efficiency (c).

TABLE 1 CPU SPECIFICATIONS

CPU	Core clock speed (GHz)	Front-side-bus speed (millions of transfers per second)	No. of cores	Per-core HyperThreading support?	L2-cache size	Supply voltage (V)	Total power draw (W)	Price (quantity)
Intel Atom 230	1.6	533	One	Yes	512 kbytes	0.9 to 1.165	4	$29 (1000)
Intel Atom 270	1.6	533	One	Yes	512 kbytes	0.75 to 1.1	2.5	$44 (1000)
Intel Atom 330	1.6	533	Two	Yes	1 MByte	0.9 to 1.165	8	$43 (1000)
Via C7	1	400	One	No	128 kbytes	0.796	9	Not reported
Via Nano	1.6	800	One	No	1 MByte	0.7 to 1.26 (1.11 on VB8001)	17	Not reported

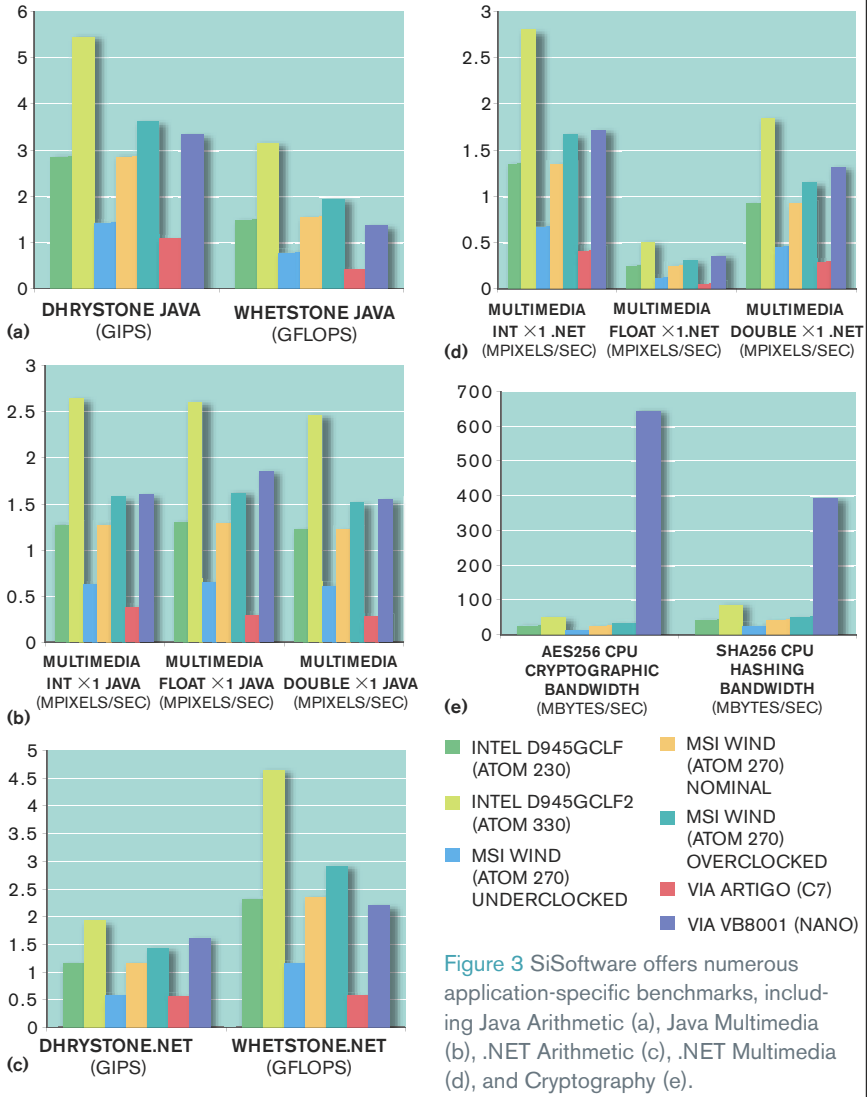


Figure 3 SiSoftware offers numerous application-specific benchmarks, including Java Arithmetic (a), Java Multimedia (b), .NET Arithmetic (c), .NET Multimedia (d), and Cryptography (e).

alized that this approach might slightly increase overall system-power consumption, but the resultant dual-bank arrangement might also make overall system-memory performance better than that of the single-DIMM alternative.

In December 2007, Via unveiled the Artigo hobbyist platform, which the company based on a pico-ITX main board housing a fanless, 1-GHz C7 CPU. Artigo is diminutive: At 3.9×2.8 in., the system board takes up less than one-quarter the area of a mini-ITX equivalent and half the area of a nano-ITX board, and its surface area is only slightly larger than that of a playing card. As with the Intel boards, Artigo has a single-slot, DDR2-533-speed interface to system DRAM; however, the board supports only 1-Gbyte-maximum memory. And, as with all of the other boards, I mated Artigo with an SSD (solid-state drive) to minimize both the overall system-power consumption and the likelihood that mass-storage-read speeds would act as a bottleneck to CPU performance.

The final contestant in this benchmarking competition was a last-minute entrant. MSI based its Wind U100 netbook, like many other manufacturers' offerings in this class, on the Atom 270, a lower-power version of the Atom 230. The Atom 270's lower power makes it suitable for battery-fueled systems, but it is otherwise identical to the 230. This system's processor normally runs at 1.6 GHz, but Version 1.09 of the system BIOS, which MSI released in late October, enables users to control CPU underclocking by 50% when the system is running on battery power, and it also allows for BIOS-defined overclocking by 8, 15, or 24%, when on ac power, using a simple two-keystroke combination.

HEAD TO THE WEB FOR THE REST OF THE STORY

As with past projects, I'll provide download links to detailed benchmark data in both text and Excel formats in an online addendum to this article. SiSoftware plans to patch the various flaws I found with Sandra Lite 2009 SP1, and I'll retest relevant hardware and post results online. I hope that, by early January, I'll have plenty of updates and other supplemental commentary to share. You'll find it all in "The price of falling prices" posts to the *Brian's Brain* blog on *EDN's* Web site at www.edn.com/briansbrain.

As has been the case in many past projects, I used SiSoftware's Sandra software. Conveniently for me, the company released Service Pack 1 of the 2009 Lite version just a few days before I began data collection. I first used Sandra's various facilities during a multihour burn-in test to ensure the stability of the overclocked system. I then subjected the MSI Wind U100 to the full Sandra benchmark barrage at 1.98 GHz, or 124%, along with 800 MHz and the nominal 1.6-GHz rate. As you assess the MSI Wind-derived data, keep in mind that this system contained 1 Gbyte of SDRAM, versus 2 Gbytes with the three mini-ITX boards. However, all of the systems ran an identical Microsoft operating-system version: Windows XP Service Pack 3—the Home version on the MSI Wind and the Pro version on the others. They all also incorporated the latest BIOS and driver versions available when I did my testing in mid-November.

In reviewing the data from Sandra's Processor Arithmetic, Processor Multimedia, and Power Management Efficiency benchmarks, the following conclusions jump out at me (**Figure 2**): First, as you would expect, given the similarities of the two CPUs, the data from the Atom 230 and 270 at 1.6 GHz is comparable, taking into account normal benchmark run-to-run variance. Second, the single-core Atom CPU's performance closely scales with operating frequency; the 800-MHz-speed underclocked results are roughly half those at 1.6 GHz, with the 1.98-GHz overclocked data roughly 24% higher than the 1.6-GHz baseline. Similarly, the dual-core Atom 330 consistently delivered roughly twice the benchmark performance of its single-core counterparts at comparable operating frequencies. Also, the geriatric C7 CPU has lower performance than the 800-MHz Atom 270, even though Via's processor operates at a 200-MHz-higher clock frequency than its Intel competitor.

The only test at which the C7 outperformed the 800-MHz Atom 270 was Multimedia Double; an analysis of the CPUs' comparative ALU (arithmetic-logic-unit)-performance data provides a potential clue to the overall disparity, and the Atom processor's HyperThreading support for limited parallel processing is another likely explanation. Conversely, Via's latest Nano CPU is a robust performer, outpacing the similarly clocked single-core Atom 230 in all benchmarks despite its lack of HyperThreading-like capabilities. On the Multimedia Double test, it even significantly sped past the dual-physical-core and quad-virtual-core Atom 330.

The conclusions for the application-tailored tests, specifically those involving cryptography and both Java and .NET virtual-machine-based algorithms, largely echo those of the earlier generic-processor tests, with the exception of a

TABLE 2 BOARD AND SYSTEM SPECIFICATIONS

Board/system	Form factor	CPU	DRAM	Mass storage	Price (one)
Intel D945GCLF	Mini-ITX	Intel 1.6-GHz Atom 230	2-Gbyte DDR2-533 Micron single-slot DIMM	Intel 80-Gbyte SATA solid-state-drive, multilevel-cell NAND	$92.48
Intel D945GCLF2	Mini-ITX	Intel 1.6-GHz Atom 330	2-Gbyte DDR2-533 Micron single-slot DIMM	Intel 80-Gbyte SATA solid-state-drive, multilevel-cell NAND	$115.98
MSI Wind	Netbook	Intel 1.6-GHz Atom 270	1-Gbyte DDR2-533 SO-DIMM	Toshiba 120-Gbyte, 5400-rpm hard-disk drive	$349.99
Via Artigo (EPIA PX10000G)	Pico-ITX	Via 1-GHz C7	1-Gbyte DDR2-533 Qimonda single-slot SO-DIMM	Sandisk 32-Gbyte PATA solid-state-drive, single-level-cell NAND	Not reported
Via VB8001	Mini-ITX	Via 1.6-GHz Nano	2-Gbyte DDR2-533 Micron dual-slot DIMM	Intel 80-Gbyte SATA solid-state-drive, multilevel-cell NAND	Not reported

TABLE 3 POWER-CONSUMPTION METRICS

Board/system	Sandra-reported CPU power (W)	Sandra-reported CPU-plus-chipset power (W)	Measured power (idle)			Measured power (peak)		
			A	W	VA	A	W	VA
Intel D945GCLF[1]	3.64	23.09, 26.73	0.31	22	38	0.4	28	48
Intel D945GCLF2[1]	3.64	23.09, 26.73[3]	0.34	24	41	0.43	31	54
Via ARTiGO (EPIA PX10000G)[1]	N/R	5.04	0.16	9	19	0.27	16	32
Via VB8001[2]	16.44	6.63, 23.07[4]	0.3	19	35	0.52	37	64

[1] Peak power consumption measured during Sandra's Cache and Memory test.
[2] Peak power consumption measured during Sandra's Processor Multimedia test.
[3] Higher power-consumption estimate reported by Sandra's Cache and Memory test.
[4] Lower power-consumption estimate reported by Sandra's Cache and Memory test.

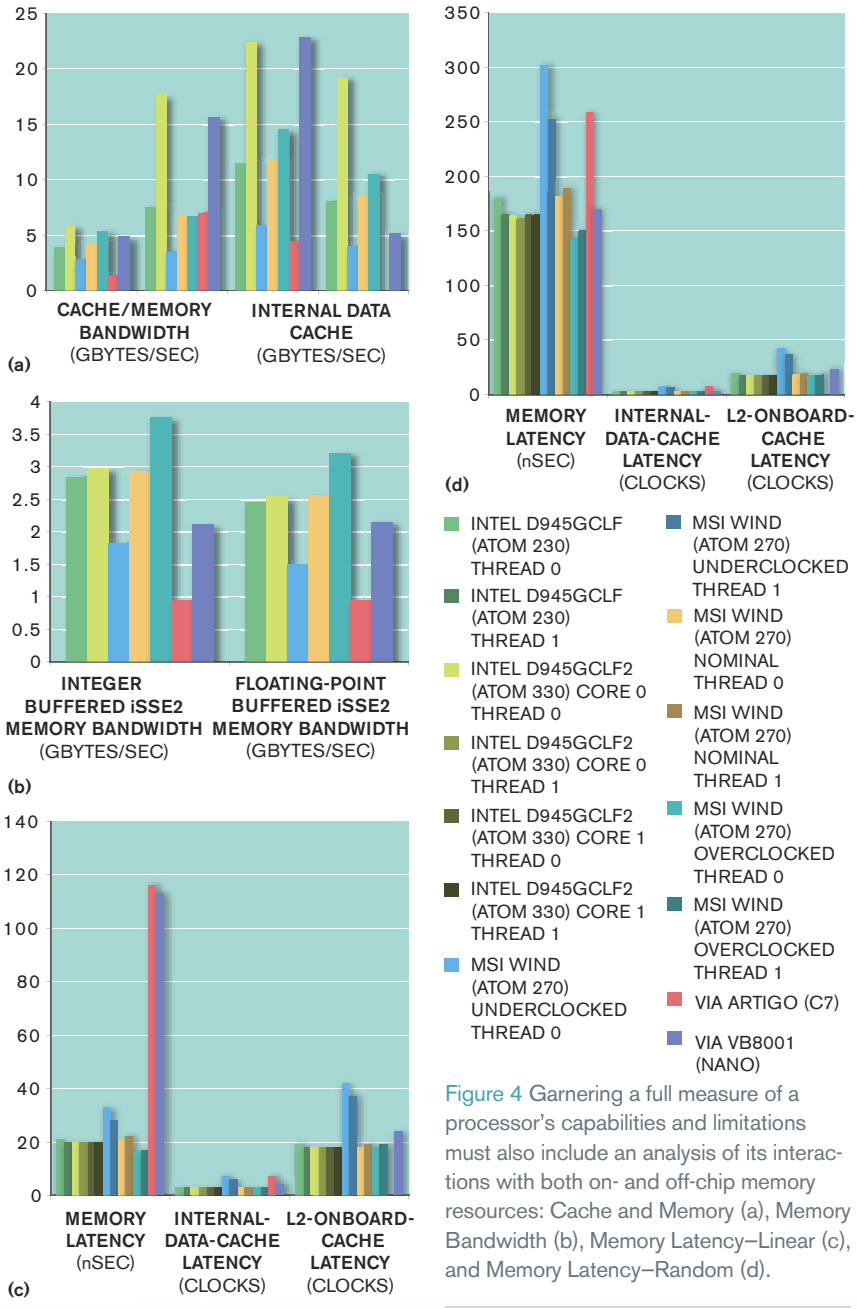


Figure 4 Garnering a full measure of a processor's capabilities and limitations must also include an analysis of its interactions with both on- and off-chip memory resources: Cache and Memory (a), Memory Bandwidth (b), Memory Latency–Linear (c), and Memory Latency–Random (d).

few key divergences that caught my eye (**Figure 3**). For example, the Via Nano CPU's earlier robust Multimedia Double capabilities did not make a repeat performance in either a Java or a .NET virtual-machine environment. Conversely, Nano performed well in the cryptography test—an expected conclusion because Via has for several product generations incorporated dedicated cryptography acceleration hardware in its CPUs. Unfortunately, a Sandra bug that I discovered—and that SiSoftware developers are now fixing—prevented me from also testing the C7 CPU with this benchmark (see **sidebar** "Head to the Web for the rest of the story").

REMEMBER THE MEMORY

Given the cache-memory configuration and capacity disparities between the various CPUs in this project, as well as the system memory-configuration and capacity disparities between the systems based on them, I felt it was important to broaden my testing beyond processor-centric benchmarks to encompass memory-inclusive studies (**Figure 4**). Looking first at the Cache and Memory test, the overall cache/memory bandwidth of

the Via Nano processor compares favorably with its Intel counterparts. However, this result is largely due to the Nano's superior L1 cache performance. Its L2 cache capabilities, conversely, lag behind those of the clock rate-normalized Atom competitors.

Note, too, that Sandra didn't report stand-alone data for Via's C7 CPU's L2 cache in either this or the Memory Latency test. "When L2 cache is equal to L1 cache, we've not found a reliable way to measure latency/bandwidth without the results being tainted by L1 cache," says Adrian Silasi, SiSoftware's lead programmer. "It is a pretty unusual configuration. Streaming to and from specific caches are really hints to the processor rather than absolute requests, and behavior varies with manufacturer and processor family."

Focusing on the Memory Bandwidth test again reveals the Via Nano's bandwidth inferiority. If you download the detailed background test data from the Web-site addendum to this article at the *Brian's Brain* blog, you'll see that this weakness extends across a suite of both integer and floating-point tests. Next, look at the Memory Latency tests. Focus first on the measured latencies for linear accesses. The Nano CPU's L1 and L2 cache performance lags behind that of Atom alternatives, but its limitations are most apparent when you look at overall memory latency. When you see the background data, you'll discover that the 256-kbyte to 64-Mbyte memory range dominates this discrepancy, again suggesting a constraint in Via's DRAM-controller design.

This conclusion is surprising considering that the Via VB8001 board employs a dual-bank, two-slot DIMM architecture and that the Nano's core-logic chip set runs DDR2-667 DRAM at full speed rather than at DDR2-533 speed. Speaking of system memory, the BIOS of the Intel boards allows users to optionally override the SPD (serial-presence-detection)-determined DRAM specifications. I used DIMMs capable of DDR2-667 speeds with the D945GCLF and D945GCLF2, so I manually entered the appropriate timings in the BIOS menus, but the boards subsequently refused to boot.

Note that the Via Nano's DRAM-latency issue was linear-access-specific; the core-logic chip set conversely delivered Intel-comparable results with random accesses. The underclocked Intel Atom 270 and the Via C7 were the underachievers in this test. I suspect that this result reflects the MSI Wind's DRAM controller's use of consistent number-of-clock settings for relevant access parameters at various system-clock speeds, even though each clock period was twice as long in the underclocked case than with nominal clock rates.

POWER PERCEPTIONS

One commonly cited criticism of Intel's Atom is that, whereas the CPU is thrifty from a power-consumption standpoint, its mated chip set is disproportionately current-hungry. You'll find corroborating evidence of this opinion in the form of the lopsided passive heat sink hovering above the core logic's north-bridge IC on one side of the CPU with the D945GCLF and D945GCLF2 boards. You'll also find it in the disparity between CPU-only and CPU-plus-chip-set power-consumption estimates from Sandra's various test results (**Table 3**). I also saw baffling evidence of it with the MSI Wind U100. I chose not to use the MSI Wind U100's statistics that P3

WHITHER AMD?

AMD (Advanced Micro Devices) declined my invitation to participate in this study, a decision that wasn't unexpected. Although I have a sound relationship with the company, it's not currently a major player in the netbook and other ultralow-cost-PC markets, reflecting the fact that the only credible products it can currently offer to these applications are aged, single- and dual-core K8 microarchitecture derivatives. However, at AMD's mid-November analyst meeting, the company unveiled the 45-nm-lithography-fabricated, dual-core K8-derived Conesus, which should debut in the first half of this year. If and when AMD's aspirations turn into shipped products, I'll request Conesus-based hardware and publish a follow-up report.

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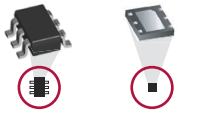

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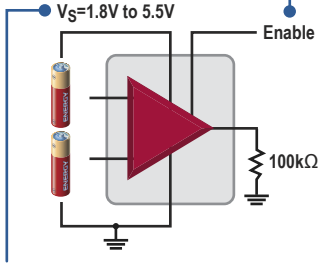

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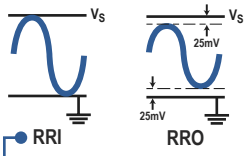

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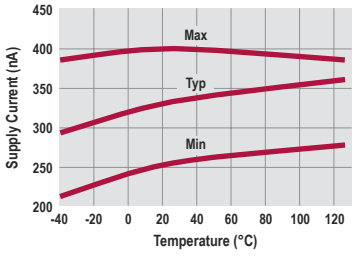

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International's Kill A Watt P4400 reported because, unlike with the other boards used in this project, they included the power consumption of the optical drive and the LCD, including its LED backlight. I will mention, however, that the measured idle-current draw of the U100 when running at 1.6 GHz, 0.54A, dropped to 0.51A when the system was under the full Sandra test load.

More generally, consider that I measured the power consumption at the ac plug, not at the CPU or, for that matter, at the dc inputs to the board. As such, my tests encompass not only the power consumption of the various components on the board, but also the inefficiencies of the ac/dc and dc/dc converters, including the nonlinearity of those inefficiencies as functions of instantaneous current draw. Speaking of statistics, part of the reason that I didn't publish Sandra's power-normalized performance data is the inconsistent CPU-plus-chipset power-consumption estimates various Sandra tests provided for the same CPU-plus-chip-set combination.

Even with those qualifiers, I still discerned some other interesting trends. Intel's D945GCLF and D945GCLF2 delivered nearly identical power-consumption results in both idle and peak operating modes, an impressive achievement for the dual-core Atom 330-based D945GCLF2, considering its notably better performance than the single-core Atom 230-based D945GCLF. Second, the Via Nano CPU-based VB8001 had lower idle-power consumption but notably higher peak-power consumption than the Intel boards. Quantifying the situation, peak-power consumption for the VB8001 was almost twice the power drawn when the board was in idle mode, whereas the peak-to-idle ratios for the D945GCLF and D945GCLF2 were 1.27- and 1.29-to-1, respectively.

Keep in mind, as you compare both the idle- and the peak-power draw of the VB8001 with that of its peers, that it employed dual SDRAM DIMM banks and that those SDRAMs ran at a 25% faster data rate than did the system memory on the other boards. It probably wasn't a coincidence that all of the single-DIMM boards drew their peak current during Sandra's Cache and Memory test, whereas the dual-DIMM VB8001 exhibited its highest power draw during the Processor Multimedia test. Finally, although the other boards I tested eclipsed the perrformance of the Via Artigo kit, any system that can consume less than 9W in idle mode and 16W in peak mode—again accounting for power-supply inefficiencies—still should earn your respect.

> For more information on the companies mentioned in this article, go to www.edn.com/090108cs.

FORECASTING FISCAL IMPACTS

Power consumption is only one of the key differentiators of raw performance; the other, price, is equally—if not more—critical. **Tables 1** and **2**, respectively, provide the published Intel prices for the three Atom CPU variants that this study evaluates, as well as those for the company's two Atom-based mini-ITX boards. Depending on your targeted application and how many CPUs you plan to buy, the price you pay might be notably less than Intel's publicly quoted price. Remember: You also need a core-logic chip set and other system building blocks. Similarly, prices for the D945GCLF and D945GCLF2 are often significantly lower than the manufacturer's suggested retail price. In mid-November, for example, the D945GCLF2 board was selling for $81.74, including free shipping, at Buy.com.

Alas, Via Technologies continues its longstanding and frustrating practice of declining to publish prices for its CPUs and boards. Internet searches reveal single-unit prices ranging from $270 to $330 for the Artigo kit, and company officials have suggested in interviews that the VB8001 will sell for approximately $180. EDN

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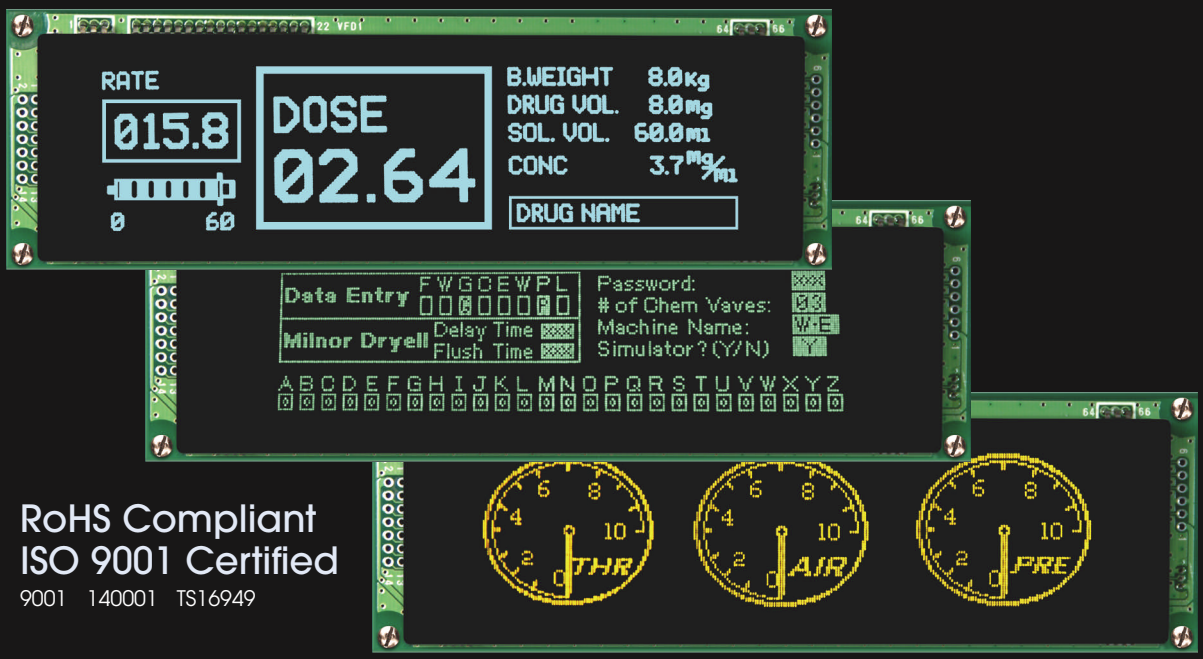

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Choosing a touch technology for handheld-system applications

THE DEMAND FOR LARGER DISPLAYS IN SMALL HANDHELD DEVICES MAKES CHOOSING THE RIGHT TOUCH TECHNOLOGY CRITICAL.

During the last two decades, touch technologies have gained acceptance in a variety of consumer applications, such as touchscreens in ATMs (automated-teller machines), track pads in laptop computers, and scroll wheels in media players. The rise of smartphones as mainstream products has brought touch technologies to mobile phones. Large displays serve a wider variety of software applications, and the overall shrinking of devices makes it critical to choose the right touch technology. A number of touch-technology options are available for handheld-device designers.

Given the prevalence of ATMs, touch technology has become such an integral part of the average consumer's life that it is nearly unremarkable. Similarly, the near-ubiquity of touch and track pads on laptop computers and scroll controls on portable media players may lull us into believing that such technology is past its prime.

However, as Apple's (www.apple.com) launch of the iPhone and Microsoft's (www.microsoft.com) announcement of Surface demonstrate, a great deal of technical innovation continues to drive touch technology as a user interface as well as a core system technology. The recent appearance of touchscreens in high-volume handheld consumer devices, such as smartphones, handheld games, personal-navigation systems, and digital still cameras, has created a new set of requirements and technical challenges for touch-technology providers, system OEMs, and software and application developers. It is helpful for designers to understand the evolution of touch technologies, the current volume drivers for touch technologies, and the emerging technological options for addressing the needs of handheld consumer devices.

Since the invention of touch interfaces in the early '70s, various technologies have emerged and have met varying degrees of success in embedded- and consumer-system applications. Technologists continue to innovate, improve, and invent touch technologies. The two leading touchscreen technologies implemented in handheld devices today are resistive and projected capacitive.

To date, the most common method of touchscreen implementation continues to be resistive touch technology. This technology is based on the simple concept of placing a small, finite gap between two conductive layers (**Figure 1**). The top layer, which the user touches, is typically a flexible clear polyester film, and the bottom layer is typically a rigid substrate made from glass. The inside surfaces of both layers are uniformly covered with a thin coating of a relatively transparent conductor, ITO (indium-tin-oxide).

A typical resistive touch panel employs a four-wire implementation. Two wires are placed on opposite edges of the touch-panel region and create a uniform voltage gradient along one axis. This is done for both the X and Y axes. The electronic controller circuit alternates applying a voltage gradient in the X direction and then in the Y direction. When the user applies pressure to the outer layer, it makes contact with the inner layer. This point of contact is measured as a voltage whose value directly corresponds to its distance from the sensor's edges. The voltage is then converted to an X- and Y-coordinate position (**Figure 2**).

The other touch technology that has received increasing attention for handheld devices is projected capacitive. This type of touch system uses either an array or a matrix of electrodes that span the touch panel's sensing region. These electrodes are typically separated from a user's touch by an insulating cover lens made from glass or plastic (**Figure 3**). When a finger touches the touch-panel surface, it changes the measured capacitance values of the electrodes closest to it. This change in capacitance can be measured by the controlling electronics, either relative to free space in an absolute capacitive system or relative to a sense electrode in a transcapacitive system. The position of the user's finger, or fingers, can be computed by measuring the changes in capacitance values of the sensing electrodes. The position of the finger, or fingers, is deter-

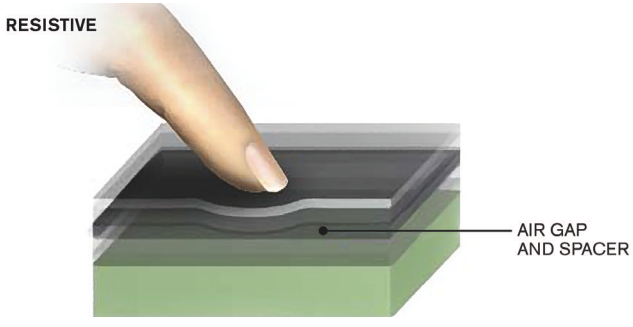

Figure 1 With resistive touchscreen technology, when you apply pressure to the outer layer, it makes contact with the inner layer, leading to an electrical contact.

mined at a much higher resolution than the electrode spacing through interpolation because the touch panel is designed so that a finger touch will change the capacitance of multiple electrodes simultaneously, not just one at a time.

There are a number of other touch technologies that, though widely deployed, are much less prevalent in handheld devices for a variety of reasons. Another capacitive touch technology, surface capacitive, uses one ITO-coated surface that conducts continuous electrical current across its surface. Manufacturers typically place this coated sensor panel beneath a very thin hard coating for durability, as ITO is very fragile. When a user places his finger on the glass panel, the capacitance of the human body alters the reference capacitance of the sensor panel. Measurements at each corner of the sensor panel help calculate the distortion of the reference field and, from that calculation, derive the X and Y coordinates of the touch point. This technology has received limited deployment in small handheld devices due to electrical implementation challenges. Furthermore, unlike project capacitive systems, in which a cover lens can protect the sense electrodes, surface capacitive systems do not work with a lens, thereby reducing their durability and ruggedness.

In acoustic touch technology, a user's touch induces a vibration, which piezoelectric transducers around the touchscreen convert into electronic signals; they in turn convert these signals into audio signals. By comparing these audio signals with the characterized library of audio signals, the technology establishes the exact location of contact.

Acoustic touch technology is ideal for large displays and is fairly insensitive to dust or scratches. Because the screen has no embedded wires, you can use a pure-glass touchscreen with inherent durability and excellent optical properties. One key disadvantage of acoustic touch technology is its inability to detect a motionless finger. IR touchscreens typically employ an array of IR photodiodes and sensors in horizontal and vertical arrays, which detect the interruption of the optical grid across the screen. When a user makes contact with the screen, the system measures the drop in the sensor-output signal; this measurement allows the system to compute the location of the touch. IR screens are among the most durable surfaces and can handle hostile environments, making them well-suited for military applications.

Last year's announcement of the Microsoft Surface has brought attention to the use of optical imaging as a touch technology. This technology uses multiple image sensors around one side of the touch surface and IR backlights on the other side. When a user places his finger on the surface, intercepting the infrared beam, the device projects a shadow. Using multiple cameras, the unit converts this shadow into a touch point through triangulation. This technique suits large surfaces and multiuser environments. Although still early in implementation, this technology promises scalability and affordability for large displays.

Engineers have long used strain gauges to measure the amount of force a user applies. Designers usually make these measurements on the platform on which the screen sits, rather than directly on the touchscreen. Therefore, such strain-gauge-based systems must account for vibration and gravity, as well as the stress that the user's contact produces. A number of newer methods of force sensing have evolved. When high accuracy is not a requirement, you can use force-sensing resistors—thick-film polymers that demonstrate a decrease in resistance proportional to the increase in applied pressure. For applications requiring high accuracy, position a capacitive-force sensor comprising two metal plates close together with a small air gap between them. Applying force on one of the plates changes the capacitance between them.

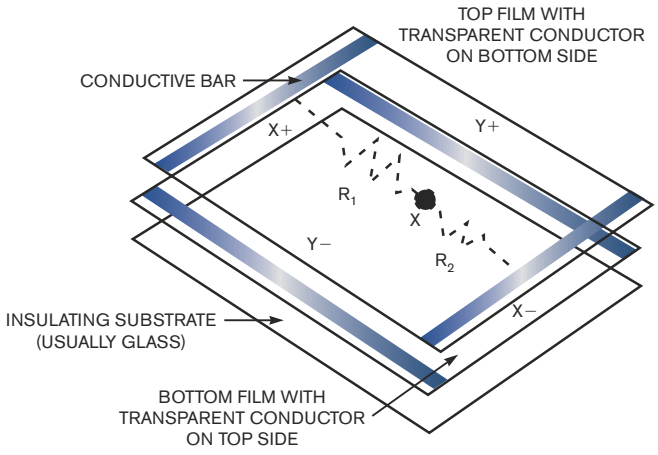

Figure 2 The most common method of manufacturing resistive touchscreens is four-wire resistive technology.

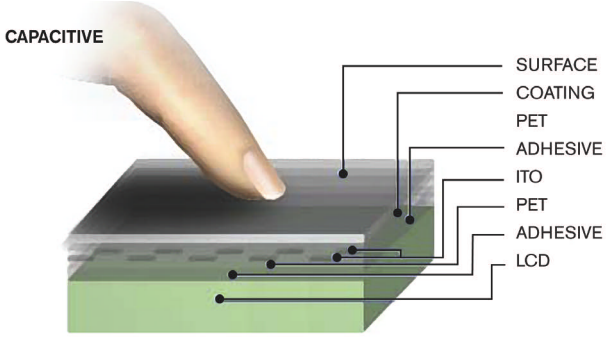

Figure 3 With capacitive touch technology, measurements at each corner of the sensor panel help calculate the distortion of the reference field and, from that calculation, derive the X and Y coordinates of the touch point.

CHALLENGES OF TOUCH TECHNOLOGY

Resistive touch has served users well during the last three decades, and resistive-touch-technology vendors have delivered continuous and sustained innovation. The resulting improvements have addressed several of the shortcomings of resistive technology, enabling it to achieve high volumes and the associated cost benefits across a range of applications. OEMs and end users benefit from the use of resistive touch technology because of its maturity, low cost, and input flexibility.

Vendors over the last two decades have derived approaches to overcome each shortcoming of resistive touch technology, so OEMs have the advantage of working with a well-characterized technology component when working with resistive touchscreens. Furthermore, advances in manufacturing tech-

nology, the maturity of resistive touch technology, and high-volume usage have made resistive touch technologies the most cost-competitive choice. In applications in which cost is critical and "good-enough" performance is sufficient, resistive touch has few peers and reigns supreme. Resistive touchscreens can use a variety of objects, including plastic or metallic styli, chopsticks, and—in a pinch—fingernails, as input devices. The only input criterion for a resistive touchscreen is that it allows you to apply sufficient force in a narrow target area, yielding flexibility in how you interact with it.

However, the mechanical wear and tear in resistive touch panels, particularly of the outer polymeric membrane, causes tiny cracks in the indium-tin-oxide coating, changing its resistance and degrading the linearity of the voltage across the membrane and therefore the measured accuracy along one axis. The mechanical nature of resistive touch devices makes them less than ideal for harsh environments. They are susceptible to moisture, and the expansion and contraction of the polymeric layer due to temperature and humidity changes can negatively affect the coatings and degrade accuracy. Users of such touchscreens experience this decrease in accuracy as drift, and the touchscreens may require recalibration. The requirement to use a bezel or well makes resistive touch sensors prone to collecting dust, and the need for a touch layer separate from the display can result in poor optical properties due to transmittance loss, reflection, and haze.

By moving beyond a four-wire-measurement approach, resistive-touch-technology vendors have tried to address issues such as the need for recalibration. For instance, eight-wire systems with four additional sensing points use voltage-gradient measurements with high sensitivity, allowing operation across a wide temperature range. They also help mitigate drift but do not address issues stemming from environmental or mechanical degradation of the outer layer. Five-wire systems, which use four wires on the substrate and use the polymeric outer layer only as a probe, are less susceptible to mechanical and environmental degradation of the outer coating. However, five- and eight-wire systems drive up the implementation cost, so manufacturers employ them primarily in nonhandheld devices.

In the early '90s, capacitive technology made its first volume appearance in notebook computers as track or touch pads and, since then, has achieved high volumes as a de facto tracking input. In 2001, capacitive touch made its first appearance in MP3-player scroll wheels and, since then, in the smartphone segment. The advantages of capacitive touch include ruggedness, design flexibility, the ability to sense more than a single finger, and an enhanced user experience.

As a solid-state sensing technology, capacitive sensing is inherently suitable for rugged environments because you can integrate it in ruggedized surfaces. The Android-based T-Mobile (www.t-mobile.com) G1, for example, integrates its sensing element underneath the cover or casing, giving it the advantage of a solid-state sensor. Industrial designs using capacitive

touch have greater flexibility because, unlike resistive touch designs, they have no bezel or case opening. The designers of the LG (www.lge.com) Prada phone used the device's surface as part of the user interface employing capacitive touch technology. Similarly, the use of solid-state capacitive technology avoids any penalty on optical clarity that a resistive touch approach would impose.

Although some vendors have demonstrated that resistive technologies can work with multiple contact points, these technologies were not designed to do so. Projected capacitive touchscreens, on the other hand, are inherently suited to multifinger use. They typically report only one point of contact as the resistive sensor averages measurements across the entire touch surface. The detection of multiple contacts, or touch points, in a capacitive touchscreen enables the multifinger-use cases, such as pinching to zoom in or out on a screen or simultaneous use by multiple users.

Capacitive sensing also offers a better user experience because the system can self-calibrate for environmental changes and is better able to adapt to environmental issues than resistive technology. The ability to use your finger instead of a stylus, as in resistive touchscreens, provides for greater user flexibility. Furthermore, the ability to use finger-based gestures, such as flicking for scrolling or dragging and dropping, is easier with capacitive touchscreens. The need to apply and maintain pressure to ensure contact in a resistive touchscreen makes the use of fingers impractical and requires a stylus to achieve the same effect as in a drag-and-drop action.

Despite its obvious benefits, projected capacitive touch technology has some disadvantages, including higher cost, software dependency, input inaccuracy, and limits on using a stylus or a gloved finger to make inputs. Many of these problems arise because the technology is in a relatively early stage of adoption. Capacitive touchscreens have yet to achieve the cost economics of resistive touchscreens and are more expensive than resistive devices. This drawback can pose a financial barrier to OEM adoption or result in higher cost for the end user.

Although capacitive touchscreens can provide a better user experience through finger-based gestures or multifinger use, such a user experience requires tight integration between the end-user interface and the underlying touch technology. This situation means that device OEMs or their suppliers of user applications must create and integrate the software necessary for such user interactions. User education and experience with such advanced features will create demand that will validate OEMs' investment in software development and integration. The release of products such as the Apple iPhone is beginning to validate these user scenarios, and, over time, this disadvantage will disappear.

The premise of capacitive technology is that the object you use as an input device, such as your finger, is conductive in nature. This fact means that you cannot use any old stylus or favorite chopstick as an input device; you instead need a special broad-tipped conductive stylus. This limitation also poses a problem when you are

wearing gloves; in that case, finger-based input becomes unpredictable or nonworking altogether. Additionally, if a user has large fingers or long fingernails, inserting input between two letters can pose a challenge. Similarly, when pecking letters or other input on screens, a finger is less precise than a pointed stylus. Although software implementations can mitigate this problem, the ability to achieve fine positioning with finger input remains a challenge. You can work around the seeming shortcomings of projected capacitive technology, especially with tight software integration and creative user-interface design.

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APPLICATION-DRIVEN CHOICES

Several factors play into the decision of which touch technology to use for a given application. These factors include the cost of the technology, the environment of the application, the size or dimension of the touchscreen itself, and the touchscreen's life cycle or frequency of use. Historically, the use of touchscreens in applications such as ATMs or information and tourist kiosks has imposed restrictions on the minimum size of the screen, the required ruggedness, and protection from vandalism or other damage. Small-screen applications, such as point-of-sale terminals, and first-generation handheld systems, such as United Parcel Service or Federal Express delivery terminals, also need durability as a key criterion for handling millions of touches without significantly degrading performance.

Similarly, the available choices of next-generation handheld systems, including smart and feature-rich mobile phones, digital still cameras, portable music players, remote controls, and handheld gaming devices, impose their own constraints on the choice of touch technology. These constraints include low power consumption for battery-powered handheld systems, cost-competitiveness, software configurability as screen sizes grow at the cost of hardware buttons, flexibility of product design for changing consumer tastes, ease of use, and a quick learning curve for consumers. For mobile phones, the ever-growing set of features, such as megapixel cameras, high-capacity audio and video storage, Wi-Fi Internet connectivity, and voice functions, demands a variety of user-input controls, even as screen real estate increases and hardware buttons become fewer.

A touchscreen system is efficient because it allows the display area in a device to serve as both an output system and an input system. A touchscreen leads to more efficient use of space in a smartphone because designers can make the display larger by eliminating the need for mechanical buttons and controls. By putting controls in a touchscreen, you can easily repurpose those controls in software to match an application's needs. This repurposing makes the device easier to use despite having a large number of functions. Controls can appear or disappear as necessary, so designers can use the display area for many purposes.

In contrast, you cannot reuse the real estate that contains the mechanical buttons. Capacitive touchscreen technology suits these devices because they require the flexibility of industrial design; ruggedness to accommodate large displays; and software configurability for superior user experiences, such as multitouch capability.

Resistive touchscreens, the workhorses of touch technologies, have during the last two decades delivered sturdy, reliable, and economical touch-based user interaction in a variety of applications. Emerging power-sensitive handheld devices, such as MP3 players and mobile handsets, rarely target single use, find use in multiple applications, and are rich in multimedia features. These devices require low-power touch technologies that allow greater flexibility for industrial designers and new user paradigms, such as multitouch and even multiuser, for system and software designers. Projected capacitive technology has emerged as the choice for the next phase of handheld designs, and optical-based technologies bear watching for future multiuser scenarios. EDN

AUTHOR'S BIOGRAPHY

Andrew Hsu, PhD, is the technical marketing and strategic partnerships manager at Synaptics. He has worked at Synaptics for 12 years, leading the company's efforts into touch solutions for handheld devices. Hsu received his doctorate and master's degrees from the University of Pennsylvania and a bachelor's degree from Caltech. You can reach him at ahsu@synaptics.com.

LINEAR TECHNOLOGY

DESIGN NOTES

Digitize a $1000 Sensor with a $1 Analog-to-Digital Converter

Design Note 456

Mark Thoren

Introduction

The LTC2450 is a 16-bit, single-ended input, delta-sigma ADC in a 2mm × 2mm DFN package, but don't let its small size and low cost fool you. The LTC2450 has impressive DC specs, including 2LSB INL, 2LSB offset and a 0.01% gain error, making it a perfect match for many high-end industrial sensors, as well as a wide variety of data acquisition, measurement, control and general purpose voltage monitoring applications.

Digitize an Accurate Sensor with an Accurate ADC

The Setra Model 270 is an exquisitely accurate barometric pressure sensor often used in weather stations and semiconductor manufacturing. A 600 to 1100 millibar input range corresponds to a 0V to 5V output. Despite its high accuracy, it does not require an expensive ADC to take full advantage of this sensor's performance. The LTC2450's DC specifications are more than adequate for the 270's 0.05% accuracy. Figure 1 shows the basic connections, and Figure 2 shows the change in barometic pressure from walking up and down a flight of stairs, taking a short break on each stair. After sample 2500, the sensor is resting on the bottom stair measuring only the change in ambient pressure. The spikes at the end of the graph are from a door opening and closing. The Setra 270 must be treated as a 4-terminal device, as the negative output is nominally 5V above the negative excitation. Figure 3 shows an isolated supply for the sensor's excitation, and the 4.7µF capacitor keeps switching noise from affecting the measurement.

Not So Obvious Features

Mixed signal designers often try to extract more resolution from an ADC by averaging samples. Averaging reduces the signal bandwidth and improves resolution, but it consumes processing resources, complicates firmware and necessitates the use of a fast ADC even though the application may require a much slower data rate. It also does not improve accuracy. The LTC2450 is inherently very accurate, and it does the averaging for you. The front-end sample rate of the LTC2450 is 3.9Msps, which is decimated to 30 samples per second by a Sinc[1] digital filter. The filter's effective bandwidth is approximately 30Hz, which means noise between 30Hz and 3.9MHz is greatly attenuated. When combined with a simple 1-pole filter, wideband noise is generally not a concern.

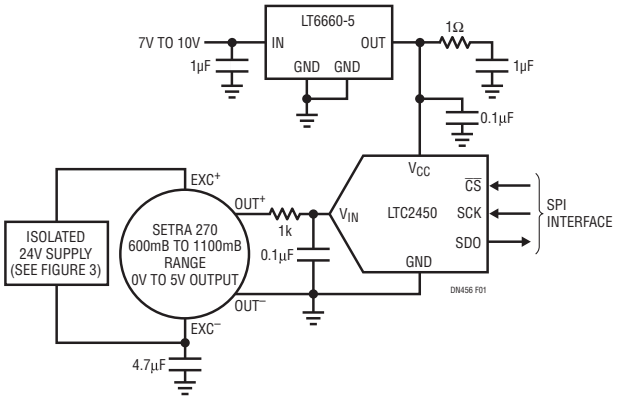

Figure 1. 16-Bit Barometric Pressure Measurement

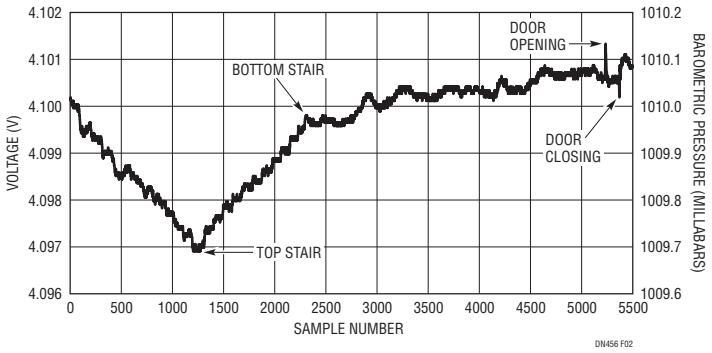

Figure 2. Stairway Pressure

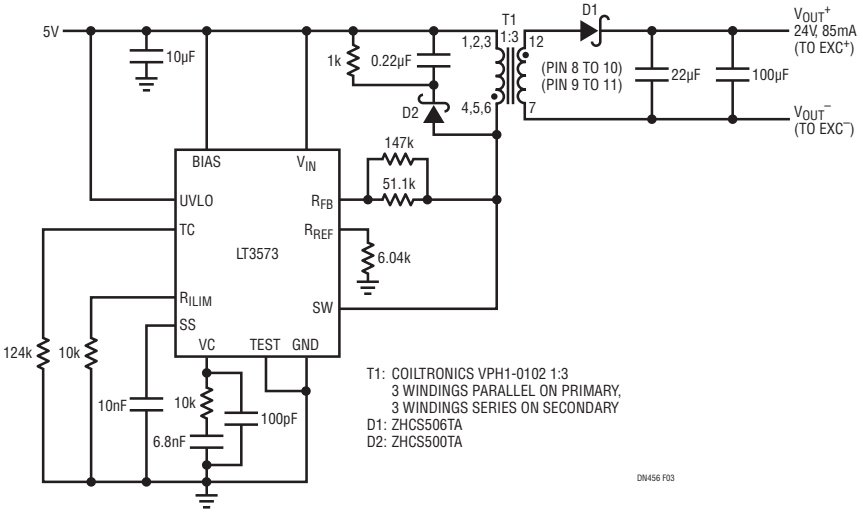

Figure 3. 24V Isolated Excitation Supply

A breakthrough feature of the LTC2450 is the proprietary modulator switching scheme that reduces the average input current by orders of magnitude compared to ADCs with similar specifications. Ordinarily, an RC filter produces offset and gain errors due to the ADC's average input current flowing through the resistor. The very low 50nA average sampling current of the LTC2450 produces less than a 1LSB error with a 1k, 0.1µF filter. This filter is more than adequate for limiting the wideband noise of most active devices driving the ADC, as well as preventing sampling current "spikes" from the modulator from affecting the source.

Conclusion

With manufacturers claiming up to 32 bits of resolution on their precision ADCs, and a confusing array of choices between 8 and 32 bits, often with highly obfuscated data sheets, where does a "medium speed, medium resolution" part like the LTC2450 fit in? It fits pretty much anywhere where you would use a 4-1/2 digit (40,000 count) digital voltmeter to test your circuit. At the other end of the performance spectrum, the LTC2450 is more economical than many 12-bit ADCs. The next time you are searching for an ADC, consider the LTC2450. It may be just what you need for performance, while occupying a tiny amount of board space that matches its tiny price ($1.15 each in 1000-piece quantities).

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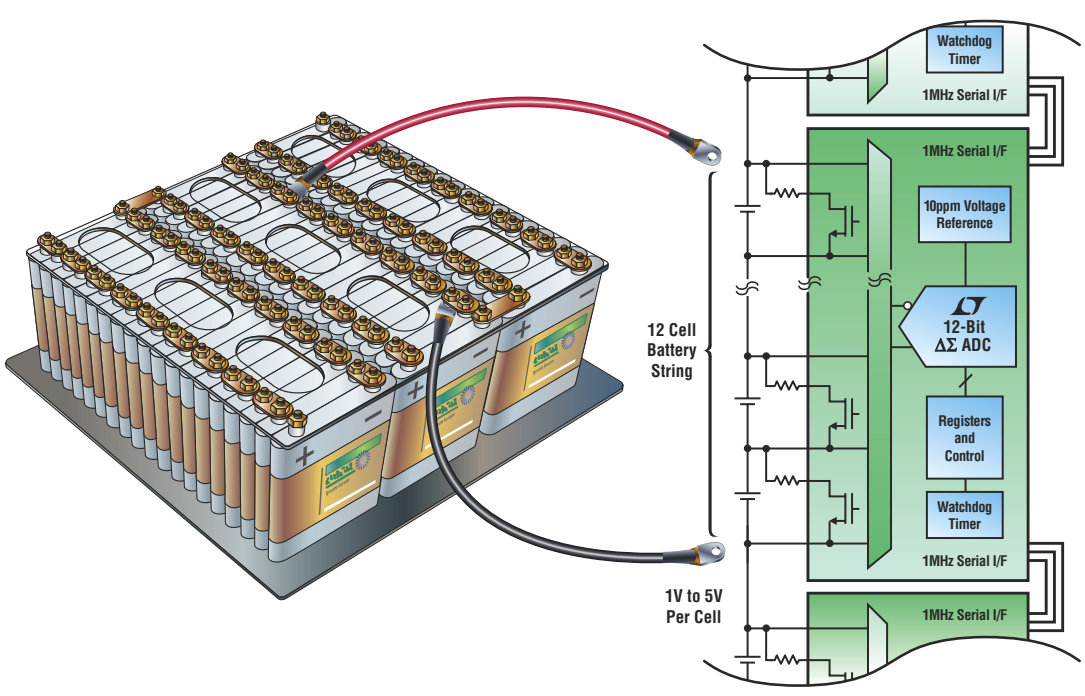

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- Diagnostics and Fault Detection
- AEC-Q100
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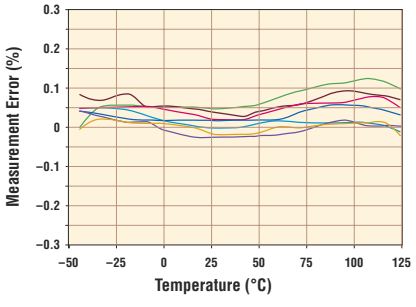
- Fully Specified for –40°C to 85°C

Cell Measurement Accuracy



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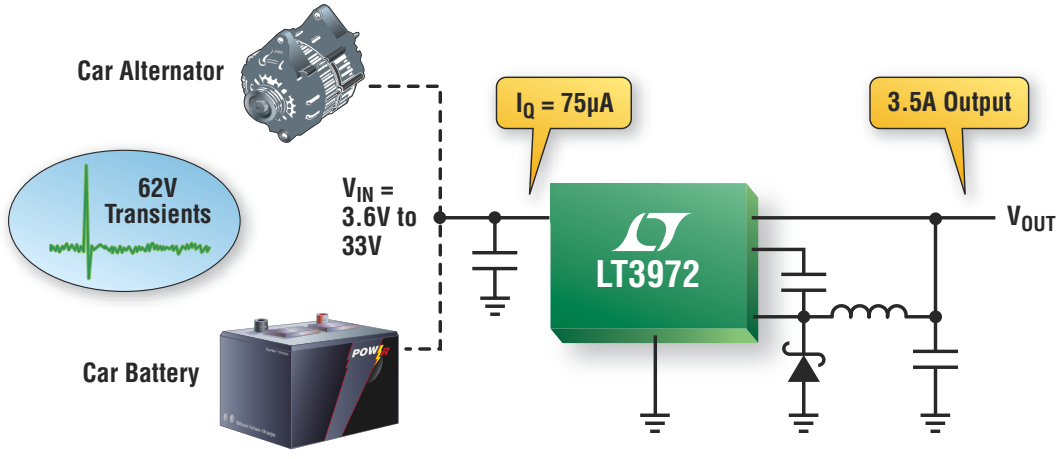

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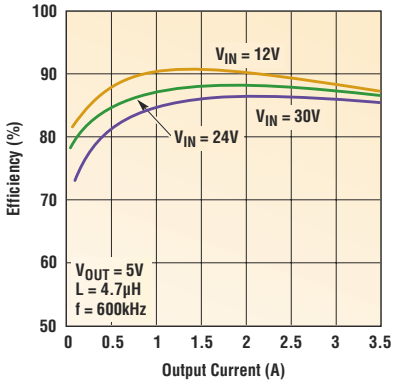
LT3682	1.0A	3mm x 4mm DFN-14

LT3972 Efficiency



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READERS SOLVE DESIGN PROBLEMS

Digitally programmable-gain amplifier uses divergent-exponential curve

W Stephen Woodward, Chapel Hill, NC

DPGAs (digitally programmable-gain amplifiers) are handy signal-processing components whenever ADCs must acquire signals with a wide dynamic range. Without the ability to accommodate input-signal amplitude to match and efficiently use ADC span, low-level inputs may not be digitized with adequate resolution, and high-level inputs may overrange the ADC and be lost altogether.

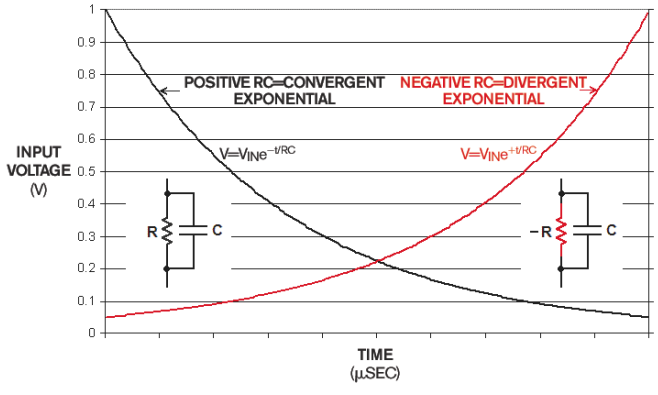

Figure 1 The behavior of the RC topology is still simple when you replace R with an active circuit that synthesizes a negative resistance.

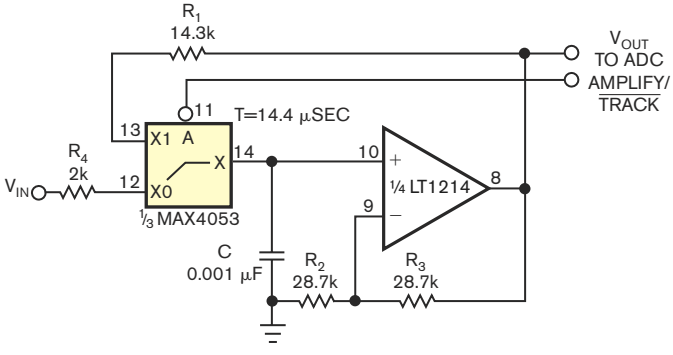

Figure 2 The divergent-exponential and negative time constants are the core concepts of the DENT (divergent-exponential-negative-time-constant) DPGA topology.

DIs Inside

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Currently available DPGA designs typically incorporate a multiplying DAC into an op-amp-feedback loop, so that the input code to the multiplying DAC sets the amplifier's closed-loop gain. Several available monolithic DPGAs, such as Linear Technology's (www.linear.com) LTC6910 and National Semiconductor's (www.national.com) LMP8100, employ this topology. But the DPGA's digital-gain-control bits are sometimes inconvenient to provide, and these devices' output span may be inadequate, for example, to interface to ±10V ADC-input spans. Also, the resolution of these devices' available gain settings is usually coarse—for example, 2-to-1 per gain step—and their power consumption is sometimes large. In contrast, this Design Idea describes a new DPGA that employs the concept of the divergent-exponential curve.

No waveform is simpler or more familiar than the $e^{-t/RC}$-convergent exponential—the asymptotic discharge to zero of an elementary RC circuit initially charged to the input voltage, V_{IN}, in which $V=V_{IN}/2$ at $t=T=\log_e(2)RC$, $V_{IN}/4$ at $t=2T$,

$V_{IN}/8$ at 3T, and so forth. Less familiar, but just as simple, is the behavior of the same RC topology when you replace R with an active circuit that synthesizes a negative resistance (**Figure 1**). Replacing R with −R makes the RC time constant negative: −RC and the waveform function yield the divergent exponential, $V_{IN}\times e^{+t/RC}$. Then, instead of converging to zero, the waveform diverges theoretically to infinity, and $V=2V_{IN}$ at $t=T$, $4V_{IN}$ at 2T, $8V_{IN}$ at 3T, and so forth. Therefore, no matter how small the input voltage might be, you can amplify it as much as you desire to any voltage by simply waiting the right amount of time $=t=\log_2(V/V_{IN})T$ after starting the negative discharge.

The divergent-exponential and negative time constants are the core concepts of the DENT (divergent-exponential-negative-time-constant) DPGA topology (**Figure 2**). When the amplify/track-control bit goes to logic one, the two-times-noninverting gain of the op-amp follower creates a negative time constant: $-(R_1+R_{ON})(C+C_{STRAY})=-14.4$ µsec, where R_{ON} is the on-resistance of the CMOS switch, and C_{STRAY} is the parasitic capacitance surrounding C (**Figure 3**). It also creates a diverging exponential: $V_{OUT}(t)=V_{IN}\times 2^{(t/10\ \mu sec+1)}$. Thus, gain $=2^{(t/10\ \mu sec+1)}$. The 1-µsec timing resolution in the amplify-control bit provides 1.07-to-1=0.6 dB=33 steps/decade gain-programming resolution. **Figure 4** graphs the voltage gain versus the time elapsed since the track/amplify-logic transition.

Unlike monolithic PGAs, DENT uses discrete components, such as op amps and switches, so it can easily accommodate parameters such as I/O-voltage spans—negative inputs and 10V amplitudes—by choosing appropriate parts and power supplies. The accuracy and repeatability of the timing of exponential generation, ADC sampling, and RC-time-constant stability limit the practical performance of the amplifier in gain-programming accuracy and jitter. In the sample circuit, with T=14.4 µsec, 1 nsec of amplify-timing error or jitter equates to 0.007% of gain-programming error. Fortunately, the near ubiquity of programmable timer/counter hardware in popular microcontroller and data-acquisition peripherals usually makes the digital generation of a precisely repeatable amplify/track control an easy matter. On the analog side, possibilities exist for self-calibration algorithms that preserve gain-setting accuracy and relax RC-component-precision requirements, but they lie beyond the scope of this Design Idea. EDN

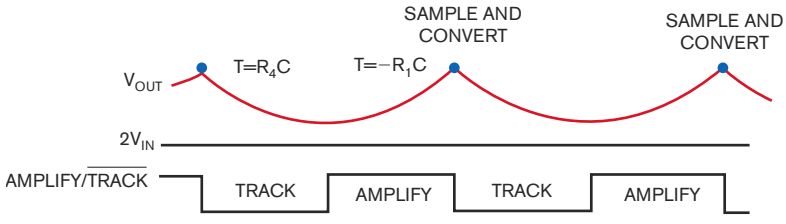

Figure 3 When the amplify/track-control bit goes to logic one, the two-times-noninverting gain of the op-amp follower creates a negative time constant.

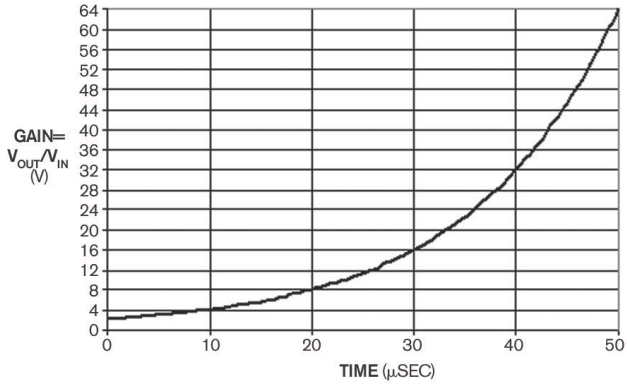

Figure 4 This graph shows the voltage gain versus the time elapsed since the track/amplify-logic transition.

Circuit indicates ac-mains-fuse failure

By Vladimir Oleynik, Moscow, Russia

Fuses are essential parts of power-distribution systems because they prevent fire or damage to electronic equipment. Fuses have the disadvantage of requiring replacement after every burnout, but they have the advantages of being inexpensive and widely available. It is difficult to determine the failure time of fuses with ceramic or sand-filled bodies to prevent arcing. This Design Idea presents a simple circuit that solves this problem (**Figure 1**). It visually and audibly indicates ac-mains-fuse failure; in most cases, audible indication is sufficient. The circuit works with a range of loads, and you can change its components to adapt to particular ac mains and load specifications.

When a fuse is in good order, the indication circuit is off because the fuse shunts it. When a fuse burns out, the indication circuit starts working. Capacitor C_1 reduces the ac-mains volt-

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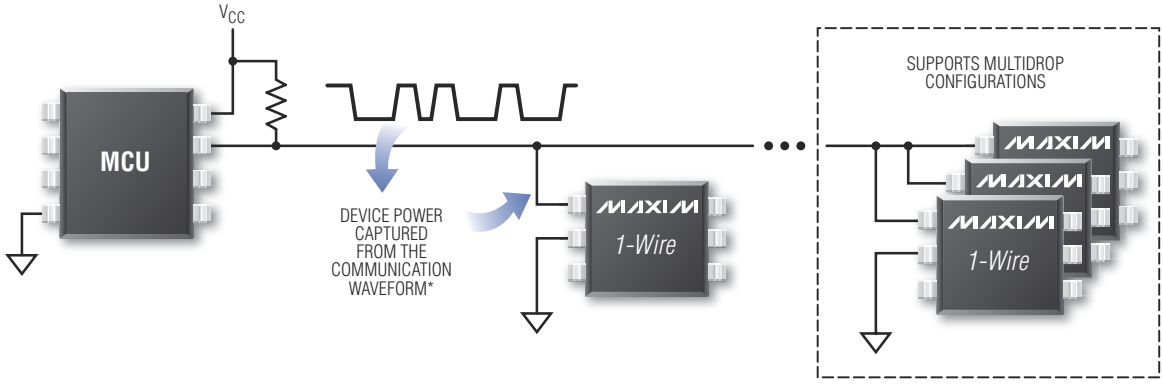

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age, and bridge diode D_1 rectifies the ac voltage. Resistor R_1 limits inrush current when capacitor C_1 is discharged. Zener diode D_2 and capacitor C_2 form a dc voltage to operate a buzzer- and blinking-LED network. The blinking LED flashes, and buzzer B_1, which has a built-in generator, sounds.

Like most other simple circuits, this circuit also has a disadvantage: It is incompatible with some load-power and ac-mains-voltage values. When a fuse burns out, the load stays connected to the ac mains, and the ac voltage divides between the circuit and the load. When the load is highly resistive or the ac-mains voltage is 110V rather than 220V, the circuit's operating voltage may be too low to drive the circuit. In that case, decrease the value of capacitor C_1 to 47 or 68 nF, after which the circuit's resistance rises. With the component values in **Figure 1**, the tested circuit operated with resistive loads of 20 to 200W. With higher-power loads, the circuit operates well because, with higher load-power values, the circuit's load resistance is lower. EDN

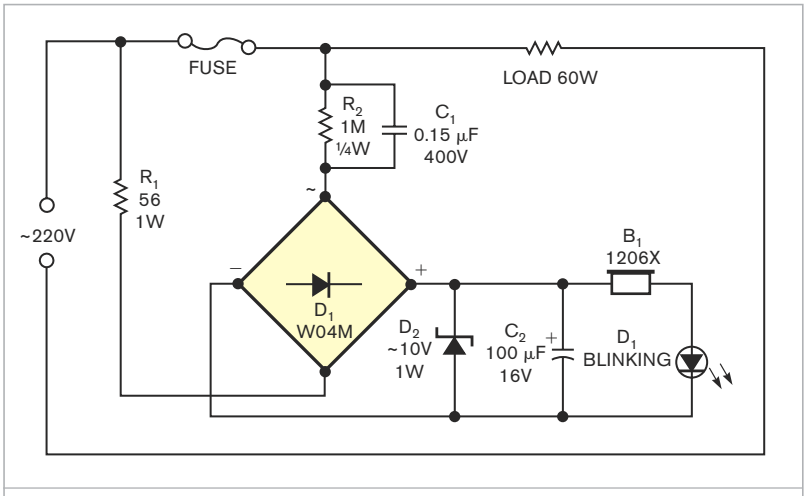

Figure 1 This circuit visually and audibly indicates ac-mains-fuse failure.

Isolation MOSFET-driver IC gets improved power efficiency at lighter loads

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

Many modern power MOSFETs reach low values of on-resistance at 5V even when the gate-to-source voltage is 5V. For heavy-duty power MOSFETS and, especially, IGBTs (insulated-gate bipolar transistors), however, engineers prefer gate-to-source voltages of 12 to 15V because the on-resistance of those power switches further decreases at higher gate-to-source voltages. The 17A-rated IRFR024 power MOSFET from International Rectifier (www.irf.com), for example, has an on-resistance of 0.075Ω (**Reference 1**). When the gate-to-source voltage is 12V, the device's on-resistance drops to 41% of its value compared to a case of a gate-to-source voltage of 5V. At a switching current of 10A, the device dissipates 6W less when the gate-to-source voltage is 12V.

IC_1, an Analog Devices (www.analog.com) ADuM5230 IC isolation driver, can boost a 5V input to a level that's high enough to drive a MOSFET's on-resistance to a low value, minimizing power dissipation (**Figure 1**). At low switching frequencies, however, the IC's high-side, internal 18V clamping dissipates the energy that the IC draws from the low-side 5V supply (**Reference 2**).

The ADuM5230's output is, however, unregulated. Fortunately, this IC has an adjustment pin that you can use to control the duty cycle of the device's internal PWM (pulse-width modulator) to reduce the duty cycle from a value of 1 to approximately 0.1. The default duty cycle has the value of 0.55 when the adjust pin is open. The lowest value of duty cycle occurs when connecting the adjust pin to the 5V supply. IC_2, an ASSR-1219 advanced photo-MOSFET device from Avago Technologies (www.avagotech.com), controls the voltage at the adjust pin. The photo-MOSFET has 0V saturation voltage between its output terminals. As a classical optocoupler has a bipolar phototransistor, using it as IC_2 would be less suitable in this case. A bipolar phototransistor has a saturation voltage of 0.4V, and, further, the CTR (current-transfer ratio) of a common optocoupler would decrease significantly when operating close to output saturation. Pulling the voltage at the adjustment pin to the external voltage-supply level comes into account when the high-side output of IC_1 has light or negligible loading.

At some point, V_{ISO}, the high-side output voltage of IC_1, will exceed the value of approximately $V_Z(I_F)+V_{FLED}\sim13.5V$, where $V_Z(I_F)$ is the voltage of zener diode D_1 at I_F, the forward current of D_2, and V_{FLED} is the minimum forward voltage at D_2, the LED of IC_2. IC_1 exceeds this value, current starts to flow through the D_2, and the MOSFET at the output of IC_2 becomes conductive. The manufacturer of IC_2 designed it for on/off operation and recommends a forward current of at least 0.5 mA (**Reference 3**).

At signal-level loading of the MOSFET at the output of IC_2, a few tens of microamperes of forward current through the LED cause the photo MOSFET's on-resistance to change

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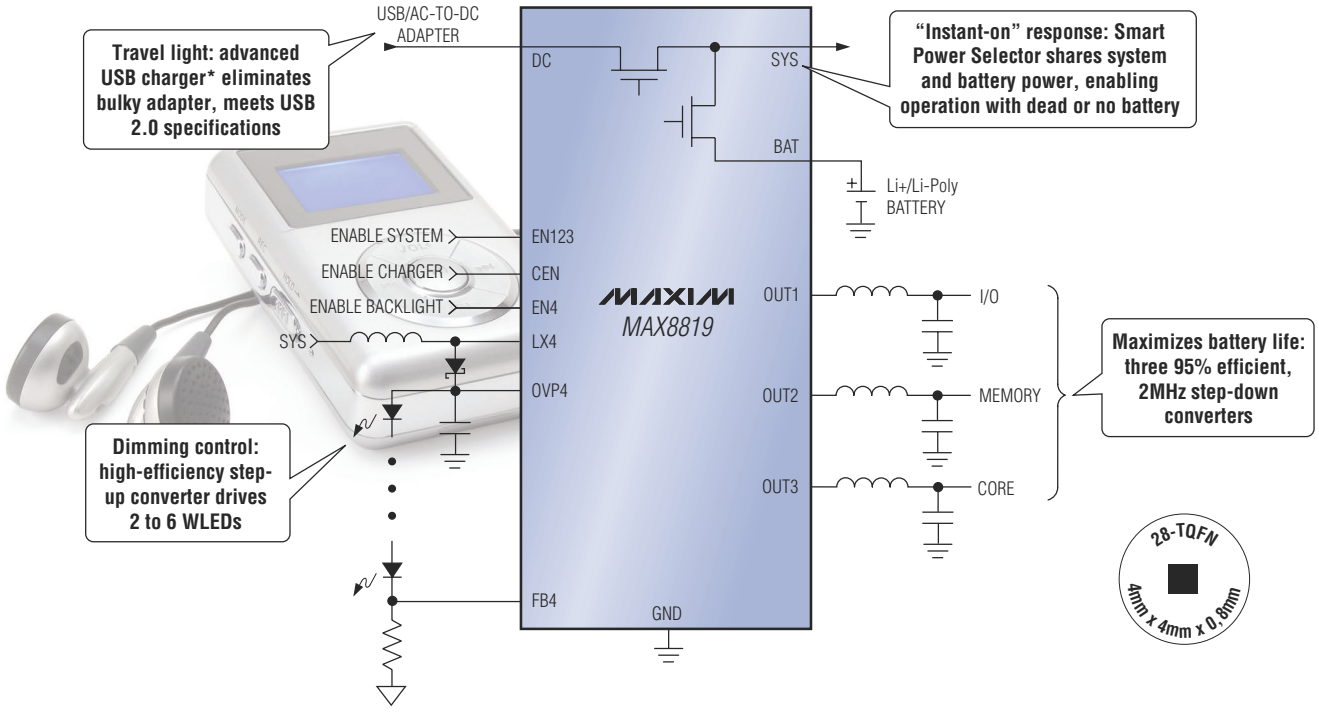
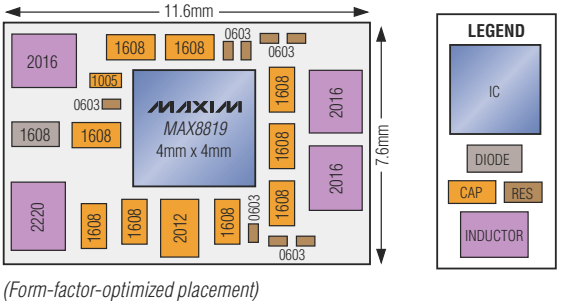
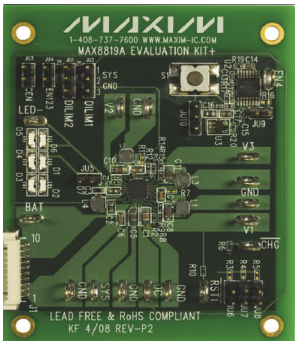


~88mm² solution area, 1mm solution height



(Form-factor-optimized placement)

Evaluation kit



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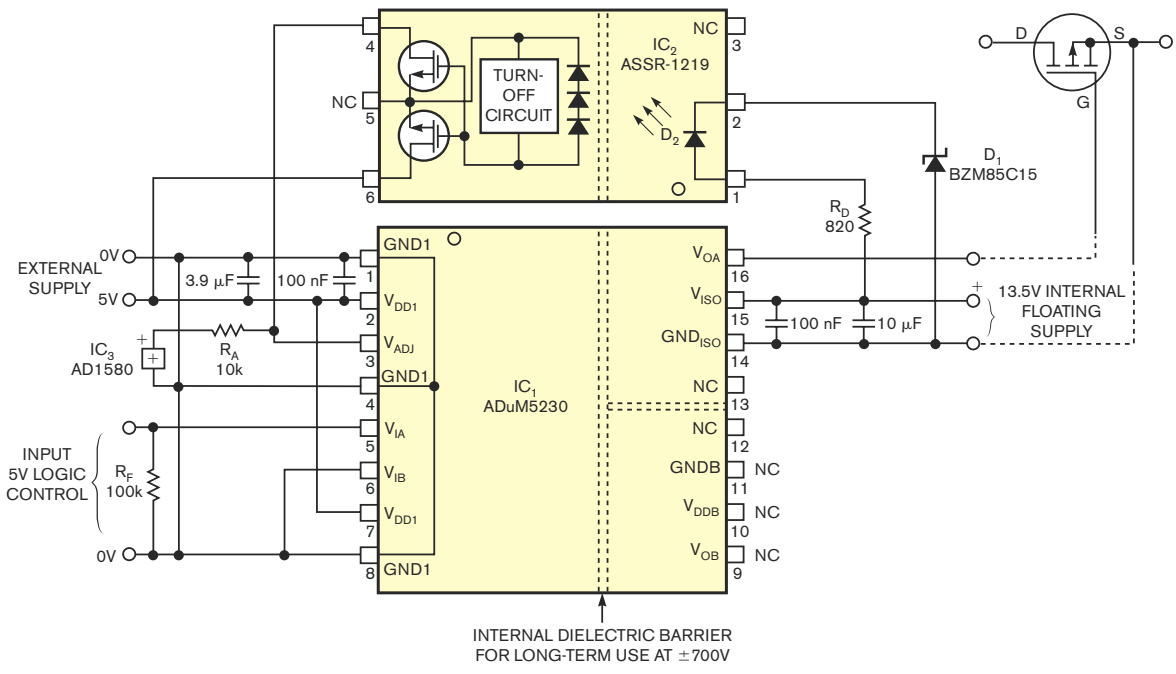

Figure 1 Connecting optical feedback by opto-MOSFET IC_2 in the power-MOSFET-driver IC_1 stabilizes the high-side output voltage to 13.5V at values of loading current down to 3.7 mA. The power efficiency of the circuit increases for a loading current of less than 7 mA.

from an almost-infinite value to a value of kilohms. The voltage level at the adjust pin then increases, and the duty factor of both the PWM in IC_1 decreases. This action establishes an isolated negative-voltage feedback. Thus, the temperatures of both the MOSFET and the LED in IC_2 have little effect on the properties of the circuit. At lighter loads, the current drain of the 5V supply is much lower than that of IC_1 with its adjust pin open.

Under test, the default supply current of the unloaded IC_1 was approximately 94.6 mA. This value decreases to 31.7 mA with the feedback in the circuit. At heavy loading, the high-side output current of IC_1 rises to approximately 20 mA, and the duty factor rises automatically to a proper value that's higher than at the default supply current. Thus, the output voltage is roughly 13.5V within the range of approximately 3.7 to 22.6 mA. The power efficiency of the circuit is 20% or greater. At an output current of 4.5 mA, the power efficiency is 20.5%, and the power efficiency for IC_1 is approximately 15%. At a current of 3.7 mA, the circuit reaches 20% efficiency, a value that's considerably higher than the 13% in IC_1 with its adjust pin open. EDN

REFERENCES

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2 "ADuM5230, Isolated Half-Bridge Driver with Integrated High-Side Supply," Analog Devices Inc, 2008, www.analog.com/static/imported-files/data_sheets/ADuM5230.pdf.

3 "ASSR-1218, ASSR-1219 and ASSR-1228, Form A, Solid State Relay (Photo MOSFET) (60V/0.2A/10Ω)," Avago Technologies, July 18, 2007, www.avagotech.com/docs/AV02-0173EN.

Synthesize variable resistors with hyperbolic taper

TL Flaig, Clinton, WA

In adjustable, frequency-selective RC networks, the reciprocal of an RC product, $\omega_C=1/RC$, determines the corner frequencies of the network. If the adjustable elements are potentiometers with a linear-control characteristic—that is, taper—$R(\alpha)=\alpha R_p$, where α is the normalized wiper position, $0\leq\alpha\leq1$, and R_p is the potentiometer's end-to-end resistance, then the corner frequencies are reciprocal functions of the potentiometer's wiper position, and the frequency scale compresses at the high end of the adjustment range. This situation is usually undesirable because it complicates adjustment of the network at the high

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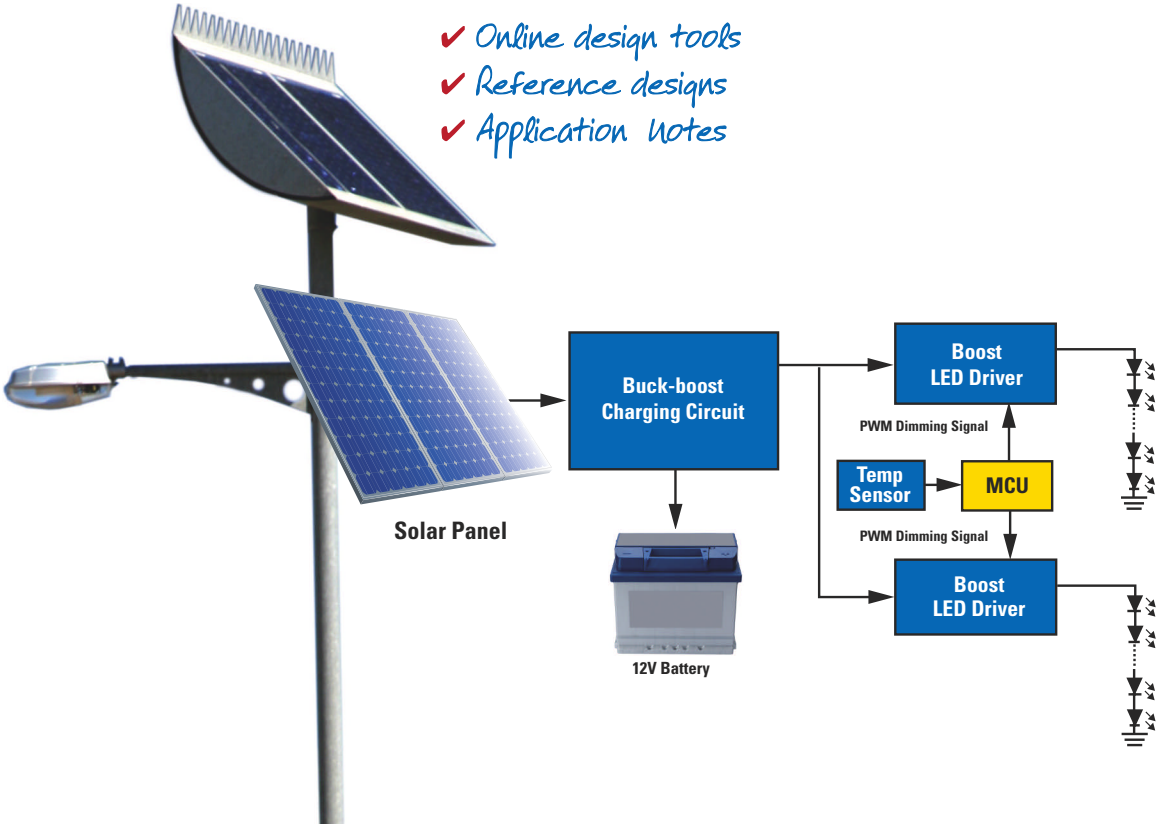

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national.com/LED

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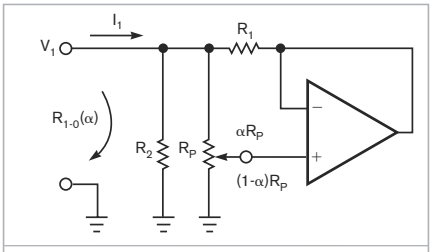

Figure 1 This simple circuit synthesizes a grounded variable resistance with a hyperbolic-control characteristic.

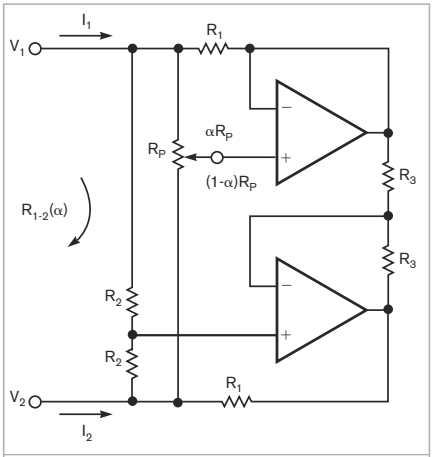

Figure 2 You can realize a floating variable resistance, with hyperbolic taper, with this circuit. Note that fixed resistors with the same number are matched pairs.

end. To make the frequency scale linear requires a control element with a hyperbolic taper—that is, something in the form $R(\alpha)=R_P/(A+\alpha B)$. Such variable resistances are not generally available from manufacturers, but you can synthesize them using a linear taper potentiometer and a few other components.

Figure 1 shows a simple circuit for producing a ground-referenced variable resistance having the desired hyperbolic-control characteristic. Analysis of this circuit yields the following relationship between the control setting and the resistance from Node 1 to ground: $R_{1\text{-}0}(\alpha)=R_1R_2R_P/(R_1R_2+R_1R_P+\alpha R_2R_P)0\leq\alpha\leq1$. If you use this resistance in series or in parallel with a capacitor, the resulting corner frequency will be a linear function of α: $\omega_C=(R_1R_2+R_1R_P+\alpha R_2R_P)/R_1R_2R_PC$. The minimum and maximum values for $R_{1\text{-}0}$ are $R_{1\text{-}0MIN}=R_1R_2R_P/(R_1R_2+R_1R_P+R_2R_P)$ and $R_{1\text{-}0MAX}=R_2R_P/(R_2+R_P)$.

To design this circuit for specific values of $R_{1\text{-}0MIN}$ and $R_{1\text{-}0MAX}$, choose $R_P>R_{1\text{-}0MAX}$ and then compute $R_1=R_{1\text{-}0MAX}R_{1\text{-}0MIN}/(R_{1\text{-}0MAX}-R_{1\text{-}0MIN})$ and $R_2=R_PR_{1\text{-}0MAX}/(R_P-R_{1\text{-}0MAX})$.

You can extend the basic circuit of **Figure 1** to produce a floating variable resistance with hyperbolic taper (**Figure 2**). The value of the floating resistance between nodes 1 and 2 is $R_{1\text{-}2}(\alpha)=2R_1R_2R_P/(2R_1R_2+R_1R_P+2\alpha R_2R_P)0\leq\alpha\leq1$, and the minimum and maximum values for $R_{1\text{-}2}$ are $R_{1\text{-}2MIN}=2R_1R_2R_P/(2R_1R_2+R_1R_P+2R_2R_P)$ and $R_{1\text{-}2MAX}=2R_2R_P/(2R_2+R_P)$. To design the circuit of **Figure 2** for specific values of $R_{1\text{-}2MIN}$ and $R_{1\text{-}2MAX}$, choose $R_P>R_{1\text{-}2MAX}$ and then compute $R_1=R_{1\text{-}2MAX}R_{1\text{-}2MIN}/(R_{1\text{-}2MAX}-R_{1\text{-}2MIN})$ and $R_2=½R_PR_{1\text{-}2MAX}/(R_P-R_{1\text{-}2MAX})$. Note that the value of the R_3 resistors does not directly affect the value of $R_{1\text{-}2}(\alpha)$. You should choose resistors that are large enough to not excessively load the op-amp outputs.

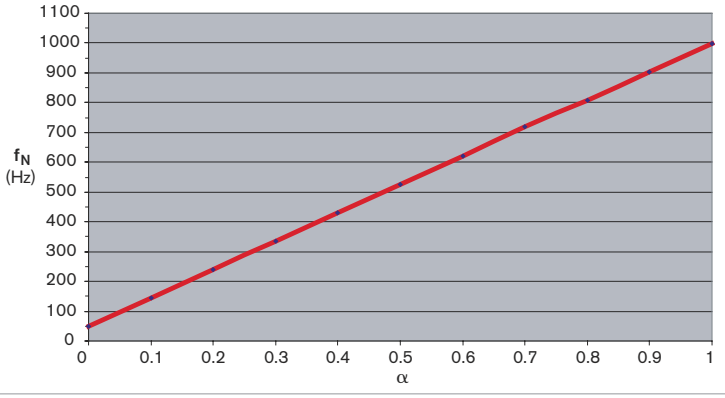

Figure 4 The Spice-simulated notch center frequency for the circuit of Figure 3 versus the normalized wiper position shows that the notch center frequency is a linear function of the control position.

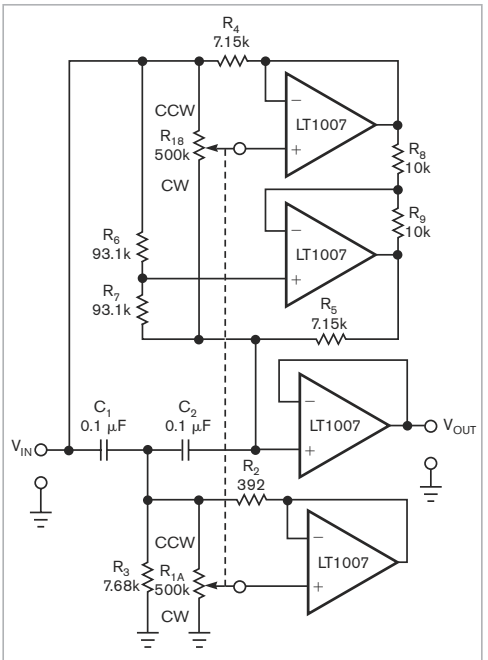

Figure 3 The basic circuits of figures 1 and 2 have been used in the design of a bridged-T notch filter with a variable notch center frequency and a linear frequency scale.

Figure 3 illustrates the application of the circuits in **figures 1** and **2** to the design of an adjustable bridged-T notch filter with a linear frequency scale. The filter has a notch center frequency that is adjustable from 50 to 1000 Hz and a notch depth of −20 dB. These requirements and the choice of 0.1-µF capacitors for C_1 and C_2 dictate that $R_{1\text{-}0}$ varies from 375 to 7503Ω and that $R_{1\text{-}2}$ varies from 6752 to 135,047Ω. (A side benefit of using this technique is that it frees the designer from the restrictions of the limited number of standard end-to-end resistance values that potentiometer manufacturers offer.)

Figure 4 plots the Spice-simulated notch center frequency for the circuit of **Figure 3** against the normalized wiper position. The notch center frequency is a linear function of the control position. EDN

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supplychain

LINKING DESIGN AND RESOURCES

Inventory management key to staying afloat in downturn

The economy is bad, but will the electronics industry see another massive downturn in 2009 similar to that of 2001? No, according to a number of electronics-supply-chain watchers, including Robin Gray (**photo**), executive vice president of NEDA (National Electronic Distributors Association, www.nedassoc.org).

"Things were on allocation [in 2000/2001], so people were double- and triple-booking and ordering, believing they could get market share from the other guy," says Gray. "Inventories were at all-time-high levels."

This time around, however, inventories are low at distributors. "Everyone learned their lesson," Gray says. "Capacity

is not building as rapidly as it did last time. The manufacturers aren't flooding the channel with more product."

The role of inventory was evident in the analog sector in late 2008. Fairchild, National Semiconductor, and Analog Devices all noted tightened ordering from distributors in the financial statements they made in the last quarter of the year. Analog Devices said that on the downturn and inventory consumption, it would reduce utilization and output of its factories.

"[Suppliers] were a lot more cautious in expanding factories' capacities," Gray maintains. "Distributors have been pretty successful in keeping their inventories pretty lean." Gray advises distribution customers and anyone who's designing to "keep a wary eye on inventory and demand. Make sure the forecasts you are getting are solid—and revivify those forecasts."

He says that a competitor can undercut any innovative product design, or it can become obsolete. "Don't be left holding inventory because you think you've got a great product and everybody is going to flock to it," he says.

GREEN UPDATE

PREMIER FARNELL TARGETS UNREGULATED E-WASTE RECYCLING IN DEVELOPING COUNTRIES

UK-based distributor Premier Farnell plc (www.premierfarnell.com) and its global sister companies, including Newark (www.newark.com), have launched an e-waste (electronics-waste) campaign to raise the awareness and tackle the dangers resulting from unregulated recycling of electronics in developing countries.

Premier Farnell says that it is commonplace to heat e-waste over open fires and strip cables and PCBs (printed-circuit boards) in acid baths to extract valuable metals, such as gold, silver, copper, and aluminum. Such actions can release toxins directly into the atmosphere, significantly impacting both the health of the recyclers and the local environment, the company says.

"It is estimated that up to 50 million tons of e-waste is discarded every year, with around 70% reaching Africa, China, and India," says Caroline Walker, Premier Farnell's group head of corporate social responsibility and environmental affairs. "Of this [waste], as much as 90% ends up with recyclers that observe no environmental or health standards."

As part of Premier Farnell's campaign, the company will lobby governments for the introduction and enforcement of protective legislation, similar to the European Union's ROHS (restriction-of-hazardous-substances) design-materials regulation and WEEE (waste-electrical-and-electronic-equipment) recycling regulation.

OUTLOOK

2009 PC OUTLOOK SLASHED

ISuppli Corp (www.isuppli.com) has slashed its 2009 forecast for PC unit shipments by nearly two-thirds and is predicting single-digit growth of only 4.3% this year. It estimates total 2009 PC shipments will reach 316 million units.

The company had previously predicted 11.9% growth for the year, followed by a 9.4% expansion in 2010 shipments. The new forecast for 2010 calls for a 7.1% growth in unit shipments. ISuppli revised its forecast in November 2008 after the financial crisis hit in the third quarter, impacting both business- and consumer-IT spending.

"The result of the financial turmoil is less money to spend, and that money itself is often more expensive," says Matthew Wilkins, iSuppli's compute-platforms principal analyst. "With less money to spend, application markets, like PCs, have been impacted. Real issues—such as difficulties in paying staff or making rising mortgage payments—are affecting businesses, as well as consumers," he continues. "The task of refreshing or acquiring new IT equipment has taken a backseat."

ISuppli estimates that desktop PCs in 2009 will suffer a shipment decline of 5%, and notebook PCs, with decreasing prices, will achieve shipment growth of about 15%.

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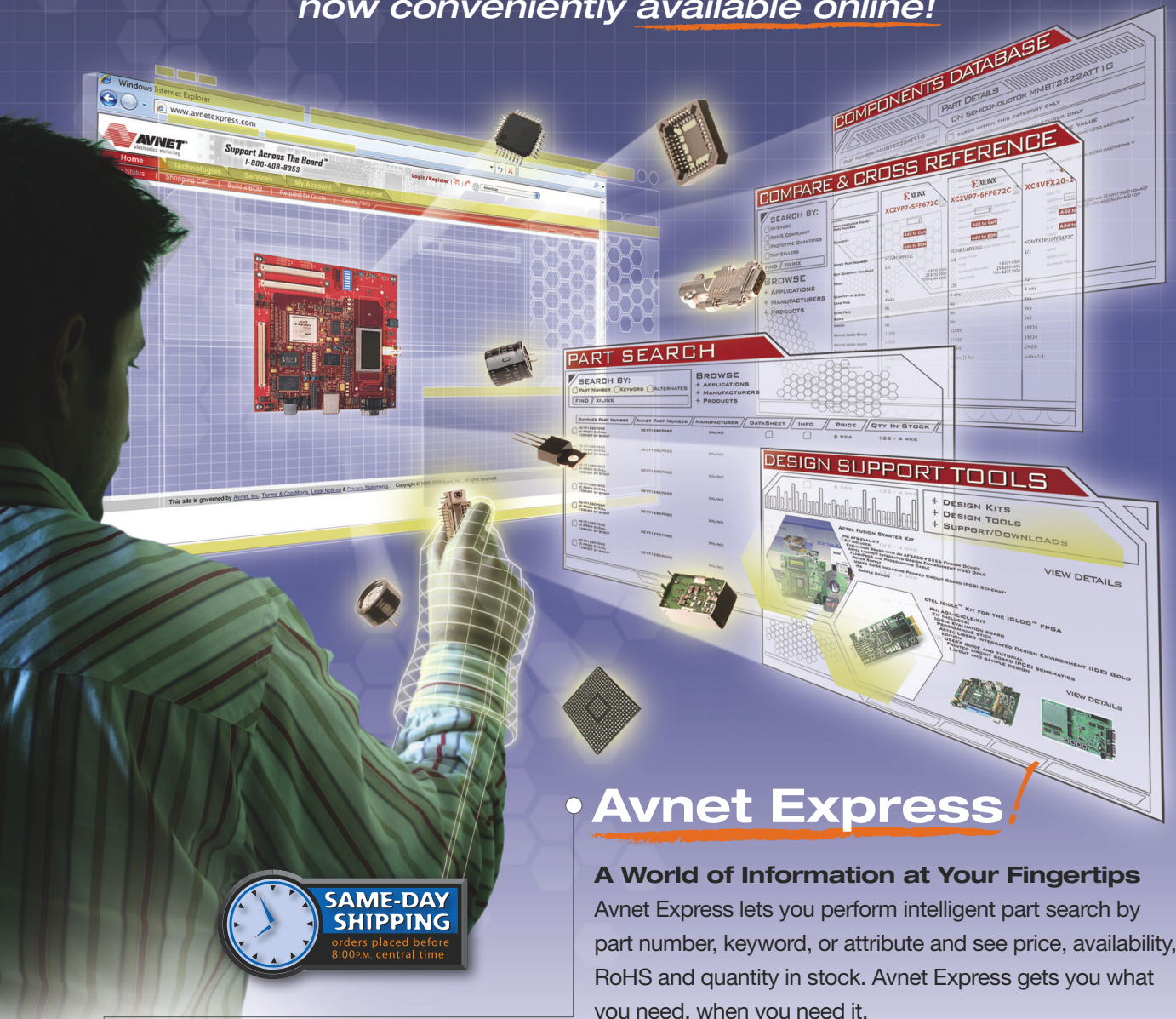

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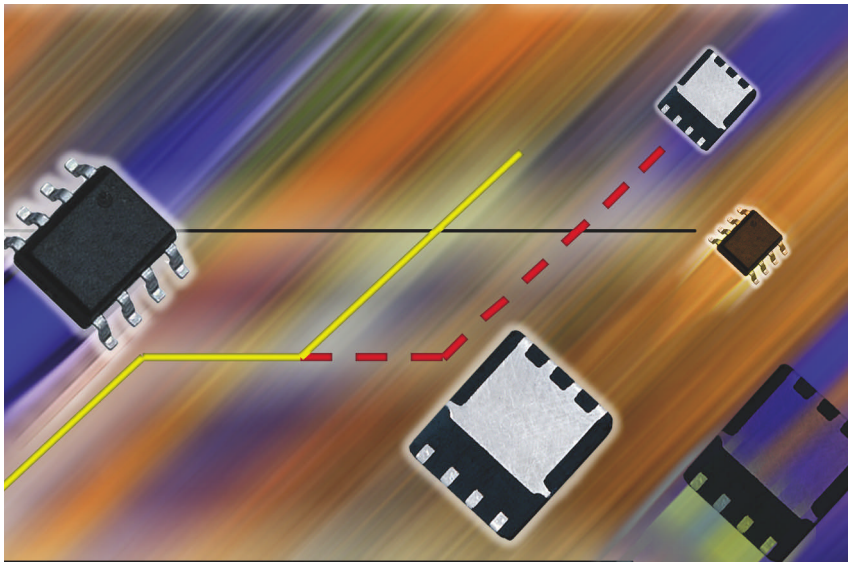

Power MOSFETs use TurboFET technology

New devices in the vendor's Gen III TrenchFET power-MOSFET line include two 20V and two 30V N-channel devices. The units have a 76.6-mΩ-nC on-resistance×gate-charge figure of merit of 4.5V and a 117.6.-mΩ-nC on-resistance-×gate-charge figure of merit of 10V. A high-side MOSFET in synchronous-buck converters saves power in notebook computers, VRMs (voltage-regulator modules), servers, and other systems using POL power conversion. The vendor claims a 45% gate-charge reduction using TurboFET technology with a charge-balanced drain structure, enabling lower switching losses and faster switching. The Gen III TrenchFETs are available in PowerPak 1212-8 and PowerPak SO-8 packages, and prices start at 32 cents (100,000).

Vishay Intertechnology, www.vishay.com

Triac photocouplers feature built-in noise immunity

The TLP3782 and the TLP3783 zero-crossing, triac-output photocouplers provide built-in noise immunity and 800V-peak off-state output voltages. Targeting office equipment, home appliances, solid-state relays, and triac drivers, the devices feature 5000V-rms isolation voltage. The triac outputs control currents in forward and reverse directions. Providing optical isolation between logic and the ac current enables improved reliability, reduced electromagnetic interference, and protection from current surges. The photocouplers consist of a gallium-arsenide infrared-emitting diode and a zero-crossing turn-on photo triac. The devices have a typical 1500V impulse-noise immunity, suiting applications with higher external noise. The TLP3782 and the LP3783 have 10- and 5-mA trigger LED current, respectively; 30-mA input forward current; and 0.1A-rms on-state current. The devices are available in DIP-6 housings, and prices range from 50 to 55 cents.

Toshiba America Electronic Components, www.toshiba.com

Snubberless triac-driver optocoupler reduces standby power

The zero-crossing FOD410 triac-driver optocoupler series eliminates the RC-snubber network when driving a snubberless discrete power triac, reducing the board space and energy required to power the circuitry. The snubberless triac optocoupler withstands high static and commutating dV/dt, protecting against the intense noise of industrial environments. Static dV/dt immunity allows the device to remain in the blocking state in the presence of voltage transients. Commutating dV/dt immunity enables the optocoupler to turn off when the load voltage and current are out of phase with each other. The optocoupler turns on only when the ac voltage is near 0V, and the device features a 10,000V/μsec minimum rating for commutating and static dV/dt. The FOD410 snubberless, zero-crossing, triac-driver optocoupler costs $1.29 (1000).

Fairchild Semiconductor, www.fairchildsemi.com

60V power MOSFETs target switching applications

Aiming at medium-voltage switching applications, the NTB5411N power MOSFET suits dc-motor drives, LED drivers, power supplies, converters, PWM controls, and bridge circuits requiring diode speed and commutating safe operating areas. The single-N-channel, 60V MOSFET features a 75A drain current and an 8.5-mΩ on-resistance, reducing power dissipation. Available in ROHS (restriction-of-hazardous-substances)-compliant, lead-free D2Pak packages, the NTB5411N power MOSFETs cost 60 cents.

On Semiconductor, www.onsemi.com

productroundup

EMBEDDED SYSTEMS

RDBMS features fault-tolerant capabilities

The Polyhedra FlashLite RDBMS (relational-database-management system) provides fault-tolerant capabilities. The flash-based embedded RDBMS offers full redundancy with instant failover and reconnection, suiting applications requiring "five-nines" (99.999%) or higher availability. The device occupies less than 1-Mbyte RAM for code and working space and can use disk or flash memory for data storage. The code is ROMable, and the cache size is controllable, allowing designers to reduce RAM usage to 200 kbytes. A Polyhedra FlashLite single-user developer license costs $11,995.

Enea, www.enea.com

VXS backplane has eight slots

Complying with the VITA 41.0 specifications, the eight-slot Star VXS backplane features a hub slot and seven payload slots in a 14-layer controlled-impedance stripline design. The backplane simulation provides strong signal performance. The 6U-high backplane has power studs in 3.3, 5, and 12V and ground on the top and bottom of the backplane, allowing flexible power option. The eight-slot Star VXS backplane costs $1500.

Elma Bustronic Corp, www.bustronic.com

Synchro/resolver or LVDT/RVDT board comes on 3U cPCI card

The DSP-based 75DS2 four-channel digital-to-synchro/resolver or digital-to-LVDT/RVDT converter comes on a 3U cPCI card. The device includes as many as four independent, isolated, programmable synchro/resolver or LVDT/RVDT-simulation channels. Each channel provides 16-bit resolution; ±1 arc-minute accuracy; and short-circuit protection output with 1.5-, 2.2-, or 3-VA drive capability. The device requires 5 and ±12V-dc power supplies and operates over 47 Hz to 10 kHz. The 75DS2 board costs $2495 (100).

North Atlantic Industries, www.naii.com

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BY SAMUEL KEREM • THE JOHNS HOPKINS UNIVERSITY, APL, SPACE DEPARTMENT

A bad-capacitor story ends happily

DANIEL VASCONCELLOS

I worked as a design engineer for an optical-telecom company that had deployed 1000 pieces of equipment worldwide. Having so many modules in the field means a trickle of returns, and it was my job to investigate the failures. One investigation taught me a wonderful lesson.

I received a module whose source of failure was easily identifiable: a charred tantalum capacitor. It failed short, making the whole multithousand-dollar module nonoperational. This surface-mount capacitor—with a 7343 footprint and 20V rating—was sitting on a 12V-dc plane. This failure rate of one capacitor in about 10,000 pieces in this time span was well below the statistical prediction. I took a picture of the fallen capacitor and considered the case closed.

In a few weeks, a customer returned a similar module with a charred and shorted capacitor in the same location. Even including this case, the failure rate was still below statistical prediction. I knew there were five more identical capacitors on the board, sitting in parallel on the same 12V-dc plane. In addition to the module's failure rate, I now had a one-in-six chance with the capacitors. So, I took another picture. I wrote a report to calm upper management, but I had a feeling that I'd better study reliability calculation in general and reliability for tantalum capacitors in particular, and the faster, the better.

In another few weeks, I received another failed module. The same capacitor looked bad. I had by now done my studying and could intimidate other people by saying long and complicated sentences about reliability, but why was it always the same capacitor? Overvoltage? Spikes? No way. The same plane contained plenty of sensitive stuff that would fry well before the capacitor even felt it. Having nothing better, I clung to the theory of excessive ripple current.

The idea of a temperature rise due to ripple current causing the failure gained traction when all three photos of the fallen capacitors revealed a common condition: almost no solder on each negative terminal. The electrical connection was still good, but there was little solder. The capacitor's positive terminal was fine with a fair amount of curvature-profiled solder. I started to promote the idea that the lack of solder had caused impeded thermal contact, but it was only wishful thinking. I calculated the worst ripple current: 10% of the maximum rating. On an operational board, I got less than 5%.

I had already dismissed other ideas—from excessive humidity to airflow turbulence. Suddenly, the picture of the layout popped up in my mind. The layout sections for the five good capacitors were identical: Vias were close to both terminals going down to an internal layer. The bad capacitor had a via at the positive terminal, but, at the negative end, there was a heavy trace going *inside* the footprint, *beneath* the capacitor, and *only then* outside. That's when I knew how to fit together all the pieces of the puzzle.

On the positive terminal, the solder stayed where it was supposed to, clinching the terminal to the PCB (printed-circuit board). On the negative side, however, during assembly, the melted solder drifted under the capacitor and solidified, lifting the negative end and bending the capacitor just enough to create a microcrack—a capacitor's well-known nemesis. I never felt as much excitement writing a technical report as I did the next day. EDN

You can reach Samuel Kerem at skerem@gmail.com. For more Tales from the Cube, go to www.edn.com/tales.

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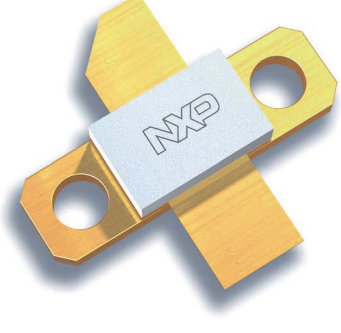

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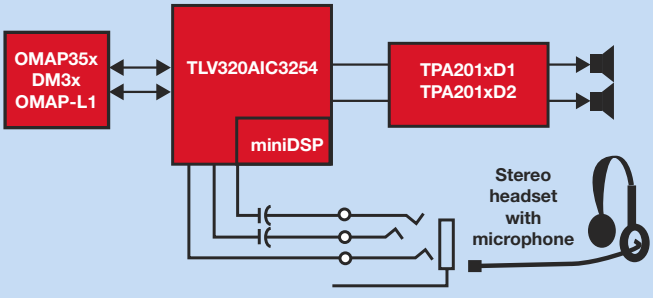
The **TLV320AIC3254** is a 1.8V low-power audio codec with an integrated miniDSP. The miniDSP offloads the host processor and allows complex algorithms such as noise and echo cancellation to run. PowerTune™ technology provides flexibility for power consumption control. The TLV320AIC3254 comes with a PurePath™ Studio Development Toolkit to enable the use of pre-defined software and the ability to customize components. **That's High-Performance Analog>>Your Way™.**



www.ti.com/tlv320aic3254
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Get datasheet, evaluation module and samples

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